EE 330
Lecture 37

Digital Circuit Design

- Basic Logic Gates
- Properties of Logic Families
- Characterization of CMOS Inverter

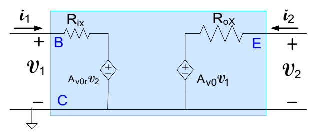
Fall 2025 Exam Schedule

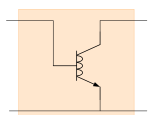
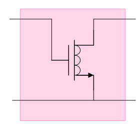
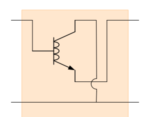
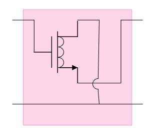
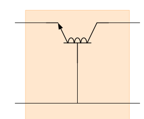
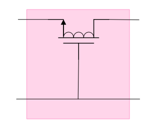
Exam 1	Friday	Sept 26
Exam 2	Friday	October 24
Exam 3	Friday	Nov 21
Final Exam	Monday	Dec 15 12:00 - 2:00 PM

Attachment to Exam 2

Basic Two-Port Amplifier Gain Table

(for low-frequency operation)

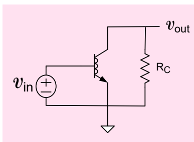
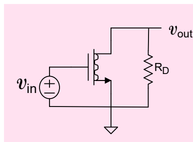
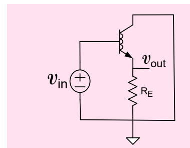
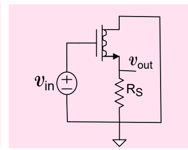
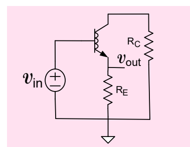
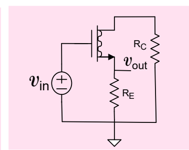
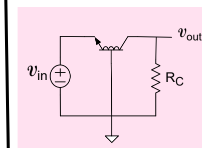
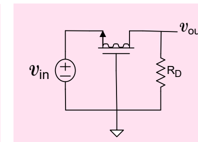
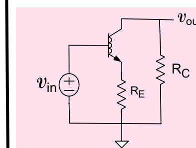
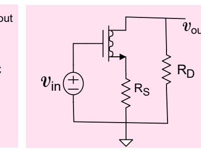


	CE/CS BJT	CE/CS MOS	CC/CD BJT	CC/CD MOS	CB/CG BJT	CB/CG MOS
						
A_V	$-\frac{g_m}{g_o}$ $-\frac{I_{CQ}R_C}{V_t}$	$-\frac{2I_{DQ}R_D}{V_{EB}}$	$\frac{g_m+g_\pi}{g_m+g_\pi+g_o}\simeq 1$ 1	$\frac{g_m}{g_m+g_o}\simeq 1$ 1	$1+\frac{g_m}{g_o}\simeq\frac{g_m}{g_o}$ $\frac{V_{AF}}{V_t}$	$\frac{2}{\lambda V_{EB}}$
R_{in}	r_π $\frac{\beta V_t}{I_{CQ}}$	∞ ∞	r_π $\beta\left(\frac{V_t}{I_{CQ}}\right)$	∞ ∞	$\frac{1}{g_m+g_\pi+g_o}\simeq g_m^{-1}$ $\frac{V_t}{I_{CQ}}$	$\frac{1}{g_m+g_o}\simeq g_m^{-1}$ $\frac{V_{EB}}{2I_{DQ}}$
R_{out}	$\frac{1}{g_o}$		$\frac{1}{g_m+g_\pi+g_o}\simeq g_m^{-1}$ $\frac{V_t}{I_{CQ}}$	$\frac{1}{g_m+g_o}\simeq g_m^{-1}$ $\frac{V_{EB}}{2I_{DQ}}$	$\frac{1}{g_o}$ $\frac{V_{AF}}{I_{CQ}}$	$\frac{1}{\lambda I_{DQ}}$
A_{VR}	0 0	0	1 1	1	$\frac{g_o}{g_m+g_\pi+g_o}\simeq\frac{g_o}{g_m}$ $\frac{V_t}{V_{AF}}$	$\frac{g_o}{g_m+g_o}\simeq\frac{g_o}{g_m}$ $\frac{\lambda V_{EB}}{2}$

Attachment to Exam 2

Basic Amplifier Application Gain Table

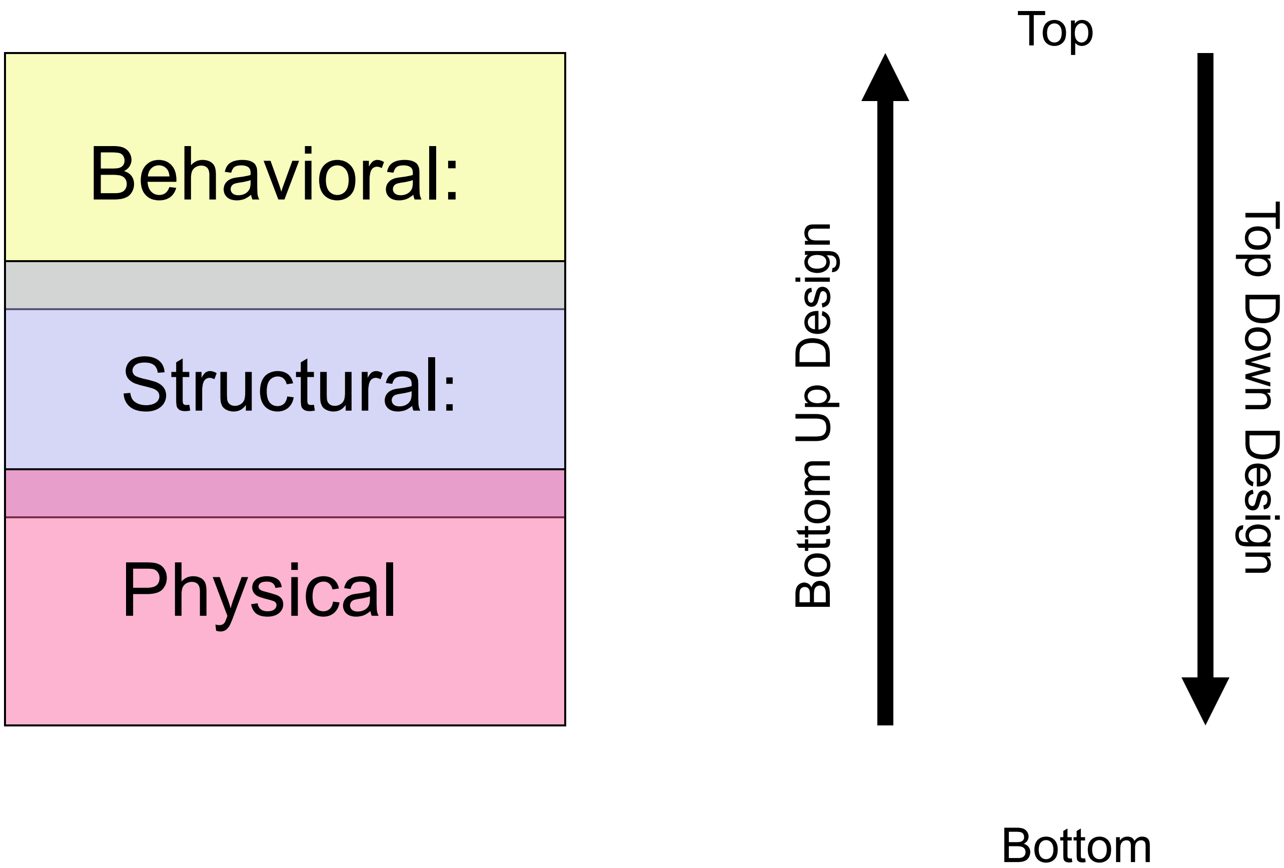
(for low-frequency operation)

	CE/CS	CC/CD	CB/CG	CEwRE/CSwRS
	BJT  MOS 	BJT  MOS   	BJT  MOS 	BJT  MOS 
A_V	$-g_mR_C$ BJT: $-\frac{I_{CQ}R_C}{V_t}$ MOS: $-\frac{2I_{DQ}R_D}{V_{EB}}$	$\frac{g_m}{g_m+g_E}$ BJT: $\frac{I_{CQ}R_E}{I_{CQ}R_E+V_t}$ MOS: $\frac{2I_{DQ}R_E}{2I_{DQ}R_E+V_{EB}}$	g_mR_C BJT: $\frac{I_{CQ}R_C}{V_t}$ MOS: $\frac{2I_{DQ}R_C}{V_{EB}}$	$-\frac{R_C}{R_E}$
R_{in}	r_π BJT: $\frac{\beta V_t}{I_{CQ}}$ MOS: ∞	$r_\pi+\beta R_E$ BJT: $\frac{\beta V_t}{I_{CQ}}+\beta R_E \cong \beta R_E$ MOS: ∞	g_m^{-1} BJT: $\frac{V_t}{I_{CQ}}$ MOS: $\frac{V_{EB}}{2I_{DQ}}$	$r_\pi+\beta R_E$ BJT: $\beta\left(\frac{V_t}{I_{CQ}}+R_E\right)\simeq\beta R_E$ MOS: ∞
R_{out}	R_C	g_m^{-1} BJT: $\frac{V_t}{I_{CQ}}$ MOS: $\frac{V_{EB}}{2I_{DQ}}$	R_C	R_C

(not two-port models for the four structures)

Can use these equations only when small signal circuit is EXACTLY like that shown !!

Hierarchical Digital Design Domains:



Review from Last Lecture

Hierarchical Digital Design Domains:

Behavioral : Describes what a system does or what it should do

Structural : Identifies constituent blocks and describes how these blocks are interconnected and how they interact

Physical : Describes the constituent blocks to both the transistor and polygon level and their physical placement and interconnection

Multiple representations often exist at any level or sublevel

Frontend design

Representation of Digital Systems

Standard Approach to Digital Circuit Design

1. Behavioral Description
   – Technology independent
2. RTL Description

   (must verify (1) ⇔ (2))
3. RTL Compiler

   Registers and Combinational Logic Functions
4. Logic Optimizer
5. Logic Synthesis

   Generally use a standard call library for synthesis

HDL

Backend design

6. Place and Route

(physically locates all gates and registers and interconnects them)

7. Layout Extraction
   - DRC
   - Back Annotation
8. Post Layout simulation

May necessitate a return to a higher level in the design flow

Logic synthesis, though extensively used, often is not as efficient nor as optimal for implementing some important blocks or some important functions

These applications generally involve transistor level logic circuit design that may combine one or more different logic design styles

Logic Optimization

What is optimized (or minimized) ?

- Number of Gates
- Number or Levels of Logic
- Speed
- Delay
- Power Dissipation
- Area
- Cost
- Peak Current

• • •

Depends Upon What User Is Interested In

Standard Cell Library

- Set of primitive building blocks that have been pre-characterized for dc and high frequency performance
- Generally includes basic multiple-input gates and flip flops
- P-cells often included
- Can include higher-level blocks
  - Adders, multipliers, shift registers,counters,…
- Cell library often augmented by specific needs of a group or customer

Digital Circuit Design

- Hierarchical Design
- Basic Logic Gates
- Properties of Logic Families
- Characterization of CMOS Inverter
- Static CMOS Logic Gates
  – Ratio Logic
- Propagation Delay
  – Simple analytical models
    - FI/OD
    - Logical Effort
  – Elmore Delay
- Sizing of Gates
  – The Reference Inverter
- Propagation Delay with Multiple Levels of Logic
- Optimal driving of Large Capacitive Loads
- Power Dissipation in Logic Circuits
- Other Logic Styles
- Array Logic
- Ring Oscillators

done

partial

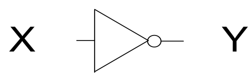
Logic Circuit Block Design

Many different logic design styles

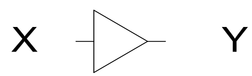
- Static Logic Gates
- Complex Logic Gates
- Pseudo NMOS
- Pass Transistor Logic
- Dynamic Logic Gates
    - Domino Logic
    - Zipper Logic
    - Output Prediction Logic

Various logic design styles often combined in the implementation of one logic block

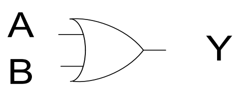
The basic logic gates



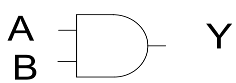
$$Y = \overline{X}$$



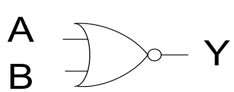
$$Y = X$$



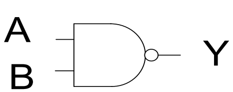
$$Y = A + B$$



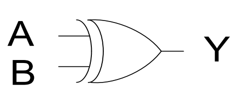
$$Y = A \bullet B$$



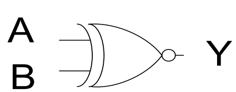
$$Y = \overline{A + B}$$



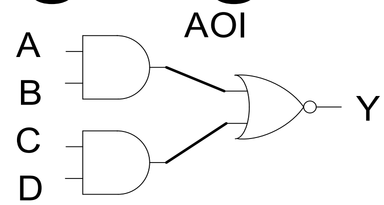
$$Y = \overline{A \bullet B}$$



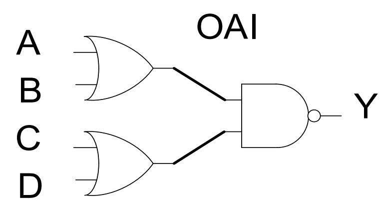
$$Y = A \oplus B$$



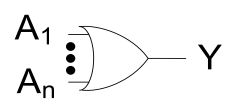
$$Y = \overline{A \oplus B}$$



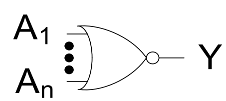
$$Y = \overline{A \bullet B + C \bullet D}$$



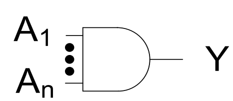
$$Y = \overline{(A + B) \bullet (C + D)}$$



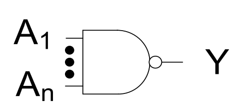
$$Y = A_1 + A_2 + \ldots A_n$$



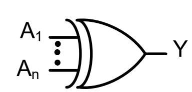
$$Y = \overline{A_1 + A_2 + \ldots A_n}$$



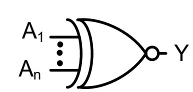
$$Y = A_1 \bullet A_2 \bullet \ldots A_n$$



$$Y = \overline{A_1 \bullet A_2 \bullet \ldots A_n}$$

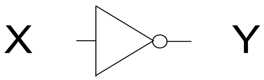


$$Y = A_1 \otimes A_2 \otimes \ldots \otimes A_n$$

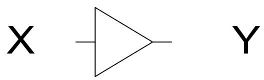


$$Y = \overline{A_1 \otimes A_2 \otimes \ldots \otimes A_n}$$

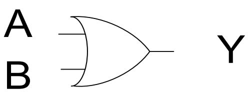
The basic logic gates



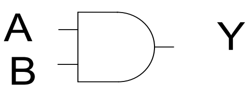
$$\mathbf{Y} = \overline{\mathbf{X}}$$



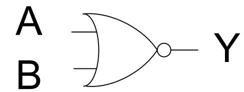
$$\mathbf{Y} = \mathbf{X}$$



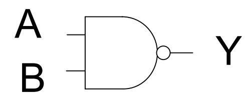
$$\mathbf{Y} = \mathbf{A} + \mathbf{B}$$



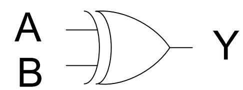
$$\mathbf{Y} = \mathbf{A} \bullet \mathbf{B}$$



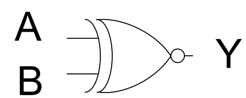
$$\mathbf{Y} = \overline{\mathbf{A} + \mathbf{B}}$$



$$\mathbf{Y} = \overline{\mathbf{A} \bullet \mathbf{B}}$$



$$\mathbf{Y} = \mathbf{A} \oplus \mathbf{B}$$



$$\mathbf{Y} = \overline{\mathbf{A} \oplus \mathbf{B}}$$

Question: How many basic one and two input gates exist and how many of these are useful?

The basic logic gates

The set of NOR gates is complete

- Any combinational logic function can be realized with only multiple-input NOR gates

The set of NAND gates is complete

- Any combinational logic function can be realized with only multiple-input NAND gates

Performance of the BASIC gates is critical!

The basic logic gates

A gate logic family can be formed based upon a specific design style for implementing logic functions

Many different gate logic family types exist

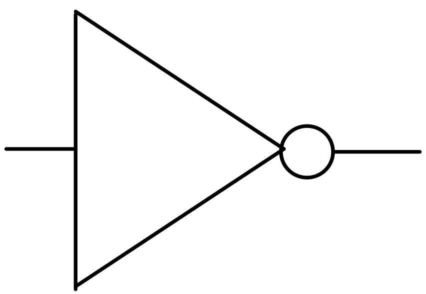
NMOS, PMOS, CMOS, TTL, ECL, RTL, DCTL,…

Substantial differences in performance from one family type to another

Power, Area, Noise Margins, ….

The basic logic gates

It suffices to characterize the inverter of a logic family and then express the performance of other gates in that family in terms of the performance of the inverter.



What characteristics are required and desirable for an inverter to form the basis for a useful logic family?

What restrictions are there on the designer for building Boolean circuits?

- None !!!!
- It must “work” as expected
- Designer is Master of the silicon !

Desirable and/or Required Logic Family Characteristics

What are the desired characteristics of a logic family?

Desirable and/or Required Logic Family Characteristics

1. High and low logic levels must be uniquely distinguishable (even in a long cascade)
2. Capable of driving many loads (good fanout)
3. Fast transition times (but in some cases, not too fast)
4. Good noise margins (low error probabilities)
5. Small die area
6. Low power consumption
7. Economical process requirements

Desirable and/or Required Logic Family Characteristics

8. Minimal noise injection to substrate
9. Low leakage currents
10. No oscillations during transitions
11. Compatible with synthesis tools
12. Characteristics do not degrade too much with temperature
13. Characteristics do not vary too much with process variations

Are some of these more important than others?

Yes ! – must have well-defined logic levels for circuits to even function as logic

Desirable and/or Required Logic Family Characteristics

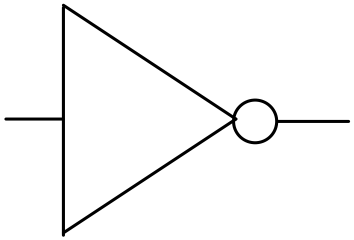
Are some of these more important than others?

Yes ! – must have well-defined logic levels for circuits to even function as logic

What properties of an inverter are necessary for it to be useful for building a logic family

What are the logic levels for a given inverter of a given logic family?

What are the logic levels for a given inverter of for a given logic family?



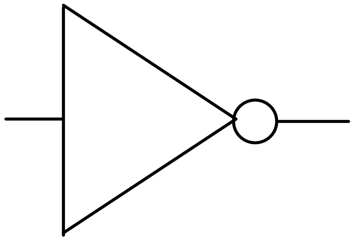
V_H=?

V_L=?

Can we legislate them ?

- Some authors choose to simply define a value for them
- Simple and straightforward approach
- **But what if the circuit does not interpret them the same way they are defined !!**

What are the logic levels for a given inverter of for a given logic family?



V_H=?

V_L=?

Can we legislate them ?

In 1897 the Indiana House of Representatives unanimously passed a measure redefining the area of a circle and the value of pi. (House Bill no. 246, introduced by Rep. Taylor I. Record.) The bill died in the state Senate.

WIKIPEDIA
The Free Encyclopedia

Main page
Contents
Current events
Random article
About Wikipedia
Contact us
Donate

Contribute

Help
Learn to edit

en.wikipedia.org/wiki/Indiana_General_Assembly

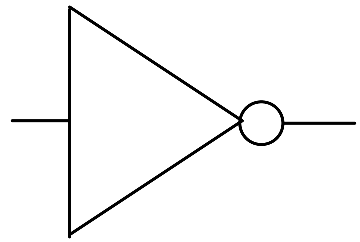
Indiana Pi Bill

From Wikipedia, the free encyclopedia

The **Indiana Pi Bill** is the popular name for bill #246 of the 1897 sitting of the Indiana General Assembly, one of the most notorious attempts to establish mathematical truth by legislative fiat. Despite its name, the main result claimed by the bill is a method to square the circle, although it does imply various incorrect values of the mathematical constant π, the ratio of the circumference of a circle to its diameter.[1] The bill, written by a physician who was an amateur mathematician, never became law due to the

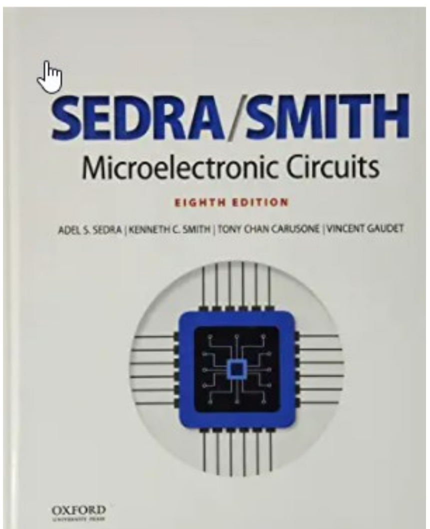
What are the logic levels for a given inverter of for a given logic family?

Can we legislate them ?



V_H=?

V_L=?



World's most widely used electronics text

Noise Margins The static operation of a logic-circuit family is characterized by the voltage transfer characteristic (VTC) of its basic inverter. Figure 10.2 shows such a VTC and defines its four parameters; V_{OH}, V_{OL}, V_{IH}, and V_{IL}. Note that V_{IH} and V_{IL} are defined as the points at which the slope of the VTC is –1. Also indicated is the definition of the threshold voltage V_M, or V_{th} as we shall frequently call it, as the point at which $v_O = v_I$. Recall that we discussed the VTC in its generic form in Section 1.7, and have also seen actual VTCs: in Section 4.10 for the CMOS inverter, and in Section 5.10 for the BJT inverter.

The **robustness** of a logic-circuit family is determined by its ability to reject noise, and thus by the noise margins NH_H and NM_L,

$$NM_H \equiv V_{OH} - V_{IH} \tag{10.1}$$

$$NM_L \equiv V_{IL} - V_{OL} \tag{10.2}$$

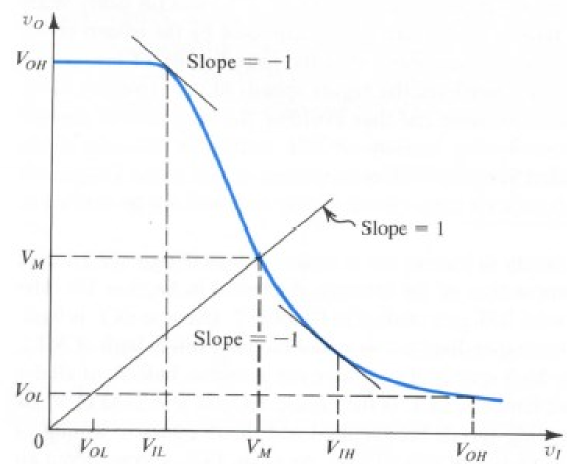
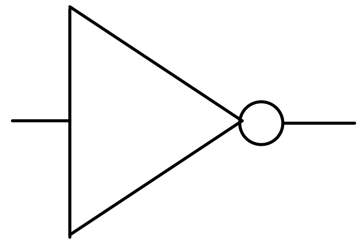


FIGURE 10.2 Typical voltage transfer characteristic (VTC) of a logic inverter, illustrating the definition of the critical points.

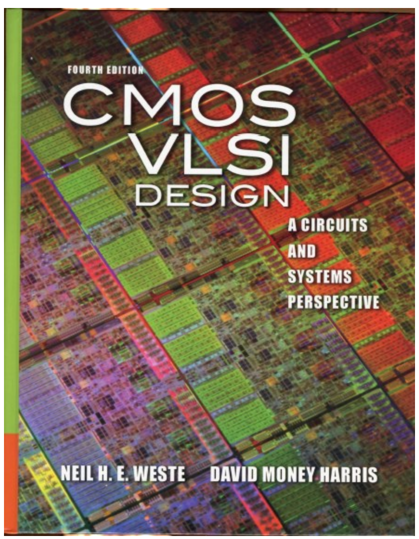
What are the logic levels for a given inverter of for a given logic family?



V_H=?

V_L=?

Can we legislate them ?



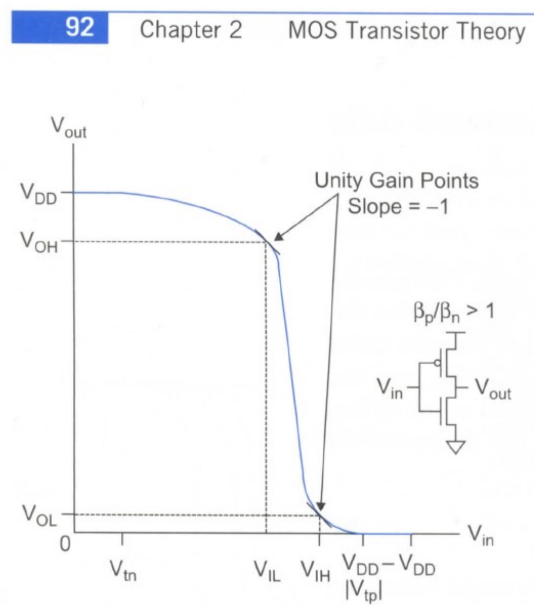
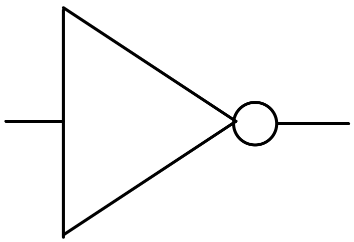


FIGURE 2.30 CMOS inverter noise margins

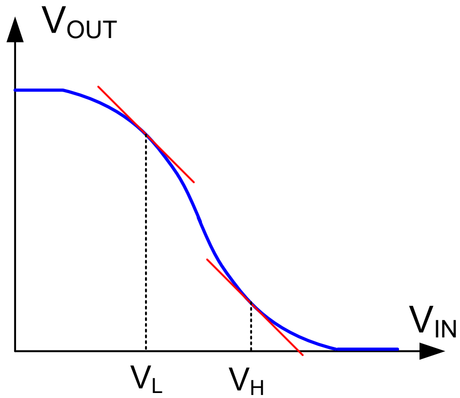
What are the logic levels for a given inverter of for a given logic family?



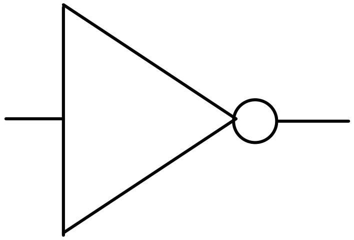
V_H=?　　　　V_L=?

Can we legislate them ?

- Some authors choose to define them based upon specific features of inverter
- Analytical expressions may be complicated
- But what if the circuit does not interpret them the same way they are defined !!



What are the logic levels for a given inverter of for a given logic family?

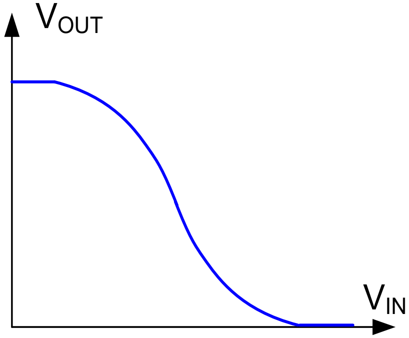


V_H=?

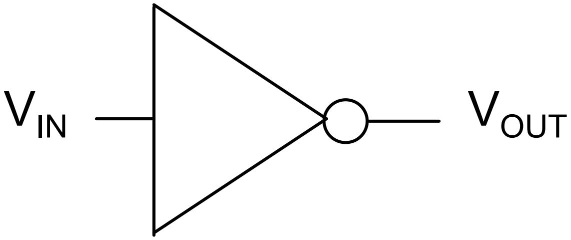
V_L=?

Ask the inverter how it will interpret logic levels

- The inverter will interpret them the way the circuit really operate as a Boolean system !!
- Analytical expressions may be complicated
- How is this determination made?

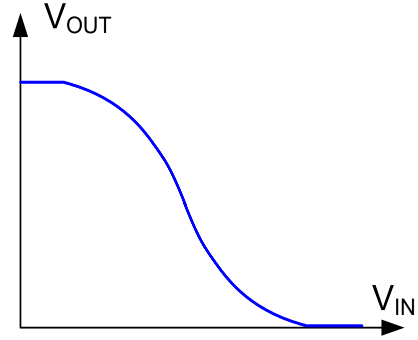


Ask the inverter how it will interpret logic levels



V_H=?

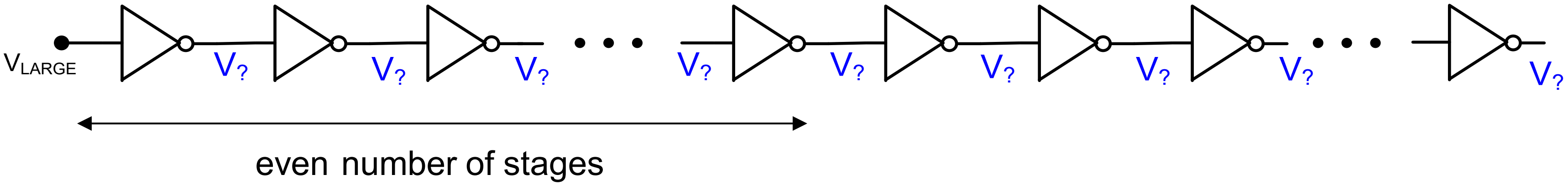
V_L=?



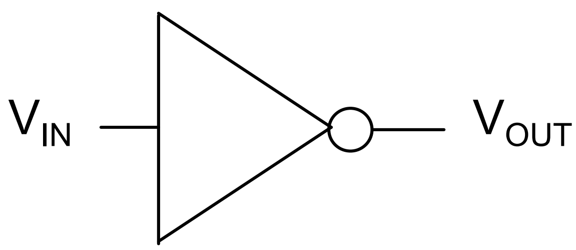
Consider a very long cascade of inverters

Apply a large voltage at the input (alternatively a small input could be used)

w.l.o.g. assume an even number of inverters in chain indicated

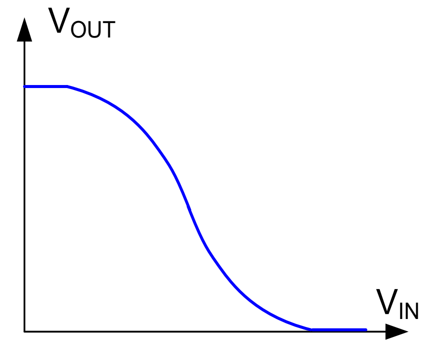


Ask the inverter how it will interpret logic levels



V_H=?

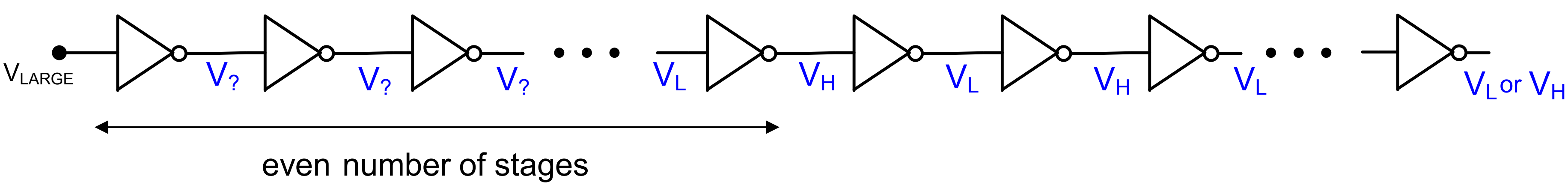
V_L=?



Consider a very long cascade of inverters

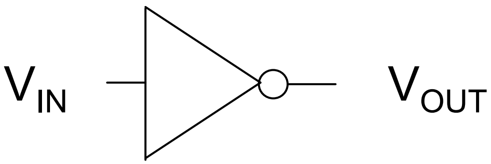
Apply a large voltage at the input (alternatively a small input could be used)

w.l.o.g. assume an even number of inverters in chain indicated



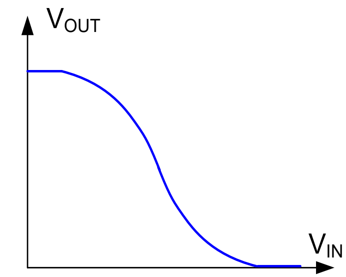
If logic levels are to be maintained, the voltage at the end of this even number of stages must be V_H, that of the next must be V_L, the next V_H, etc.
(may not be applicable for first few outputs near the input)

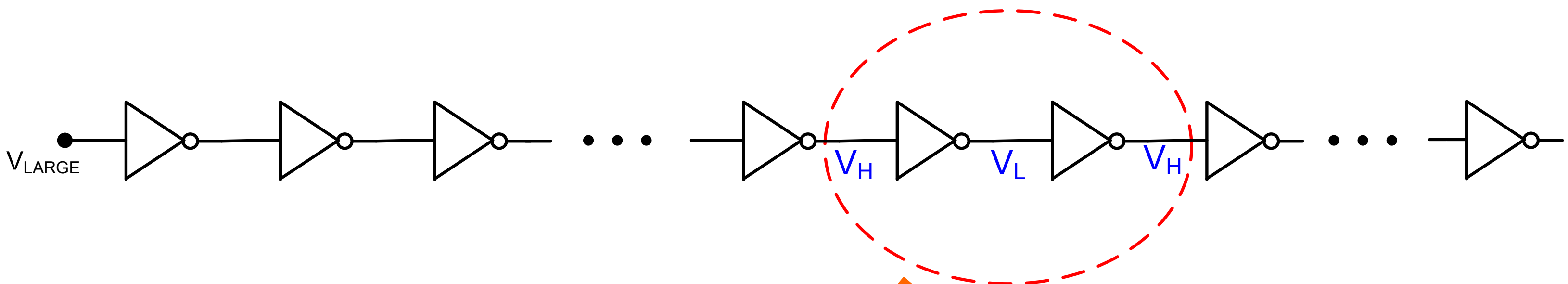
Ask the inverter how it will interpret logic levels



V_H=?

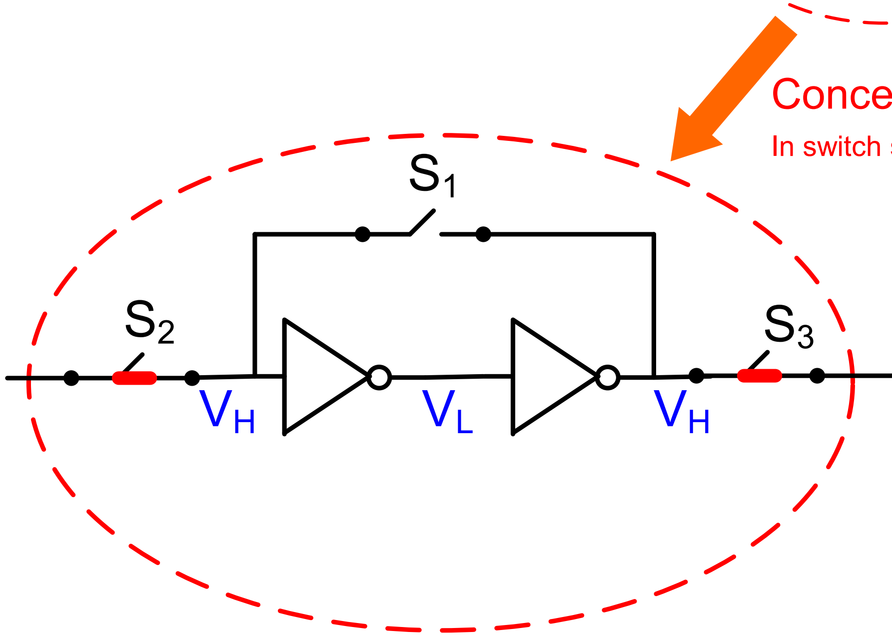
V_L=?



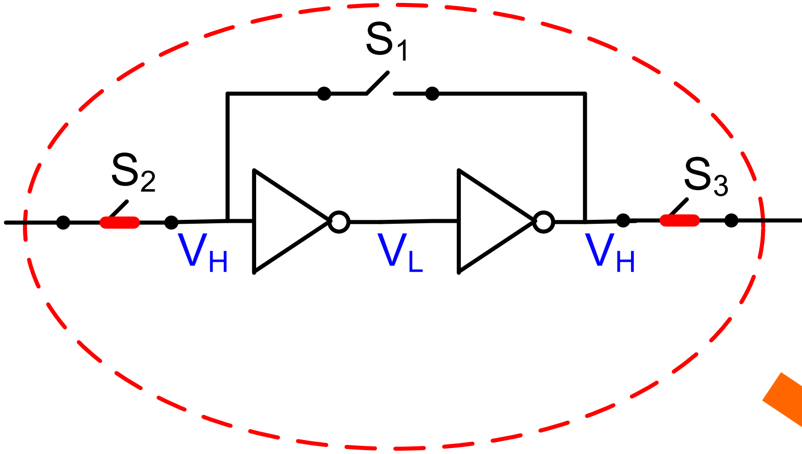


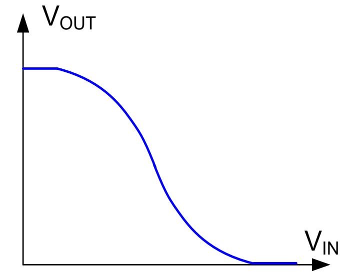
Conceptually add S_1,S_2 and S_3

In switch states shown, nothing should change



Ask the inverter how it will interpret logic levels

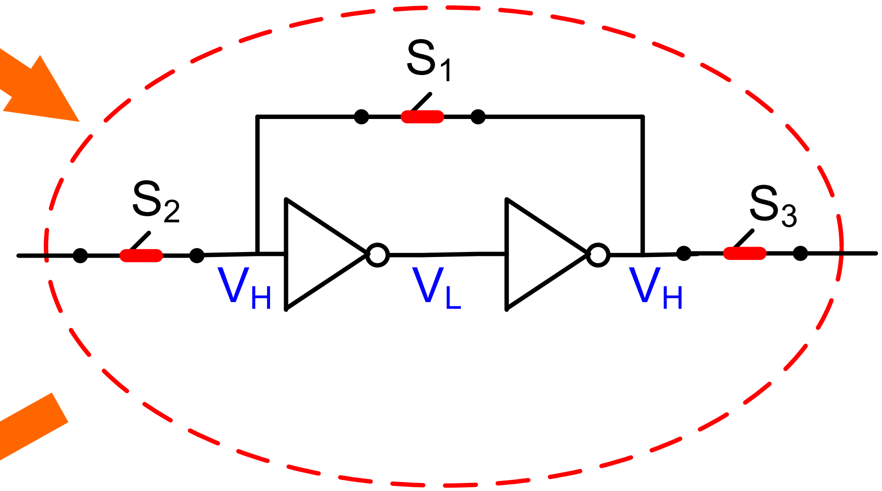


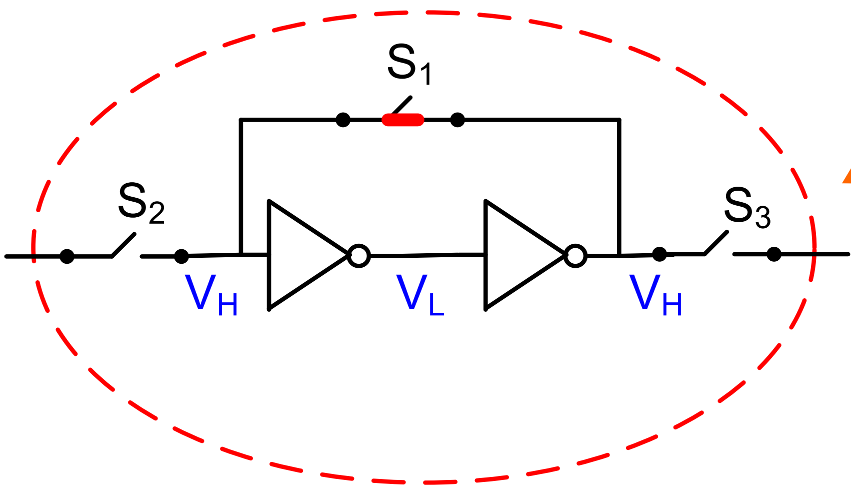


V_H=?

V_L=?

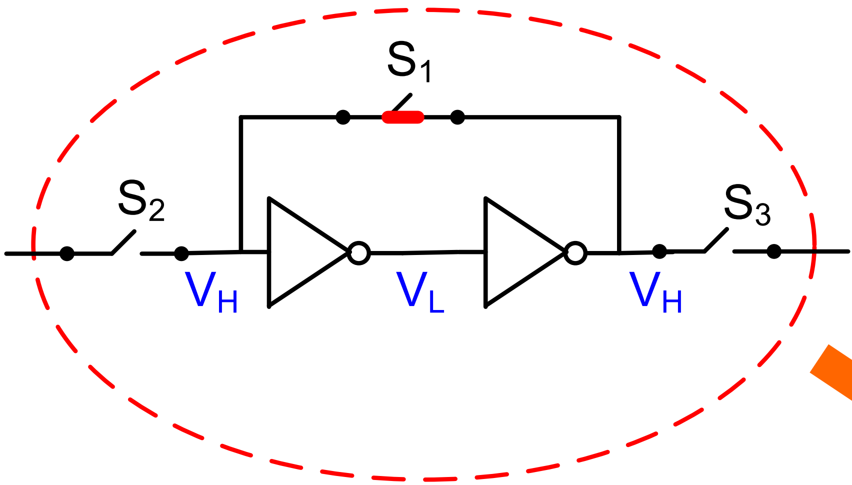
Even closing S_1 nothing should change

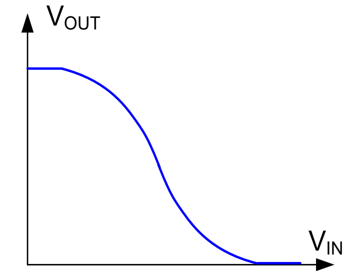




And then opening S_2 and S_3 nothing should change

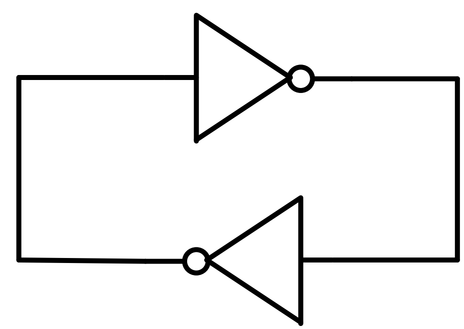
Ask the inverter how it will interpret logic levels





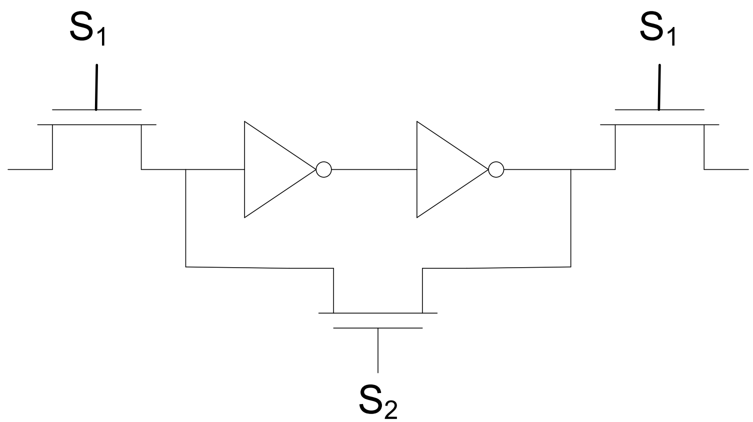
V_H=?

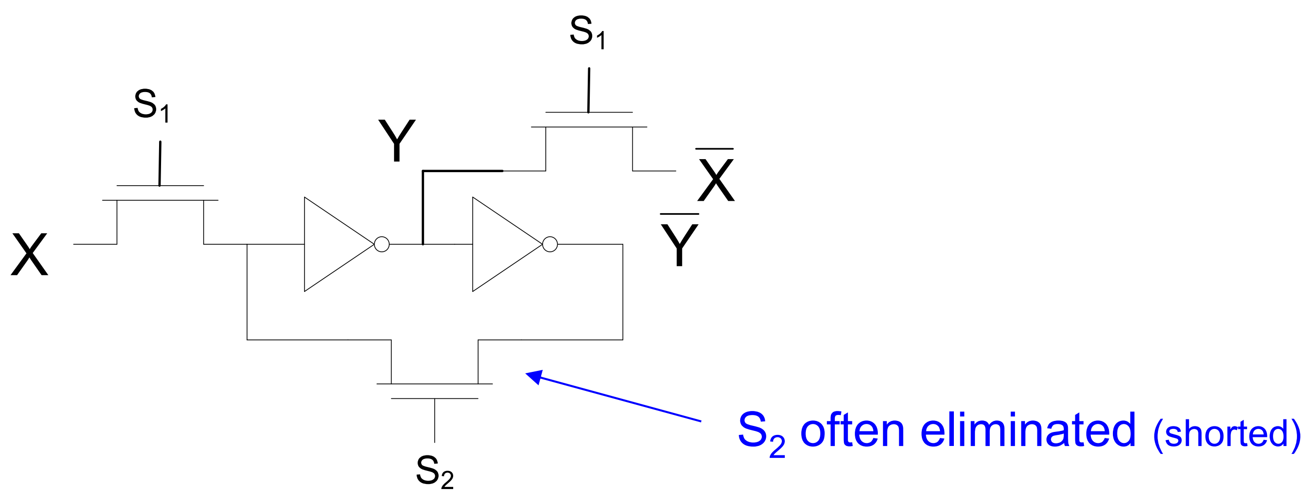
V_L=?



- Two inverter loop
- Very useful circuit !

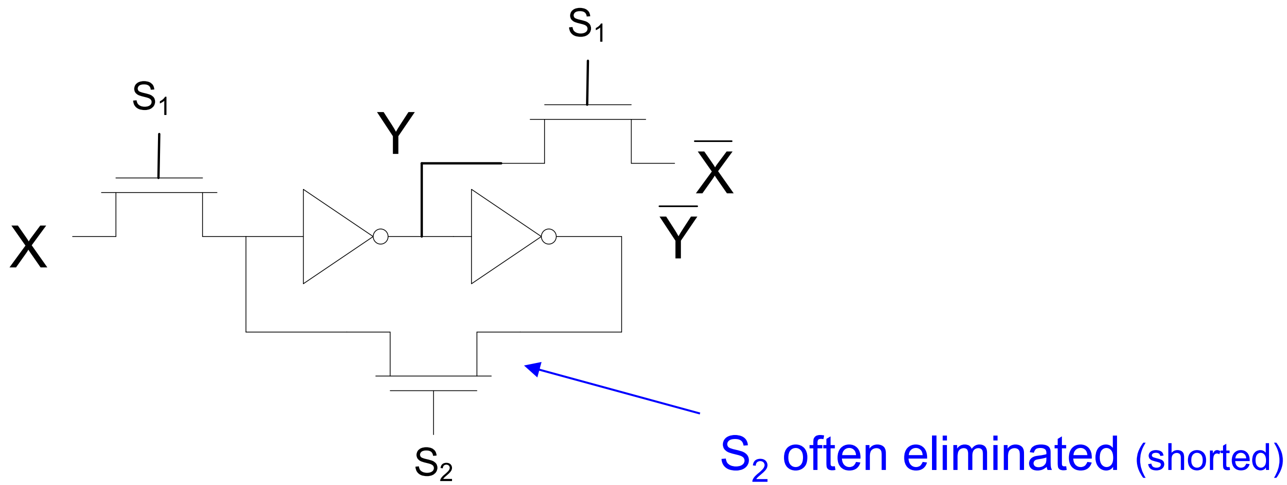
The two-inverter loop

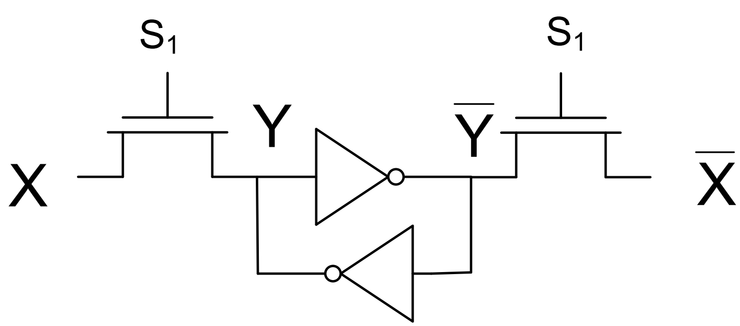




SRAM Cell

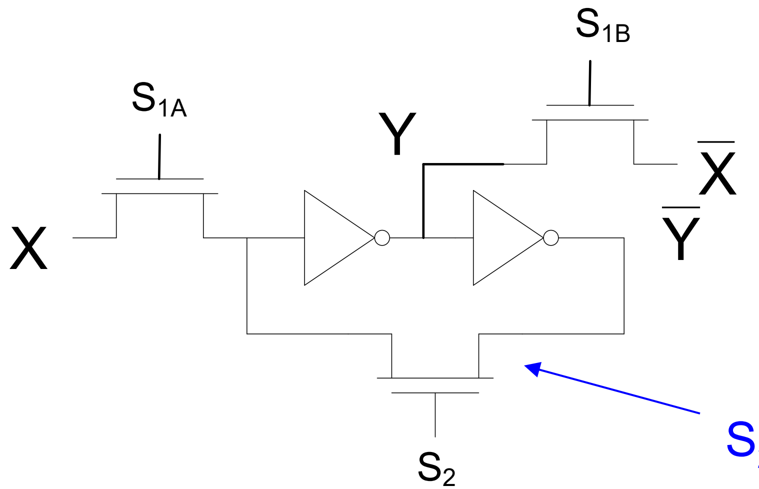
The two-inverter loop





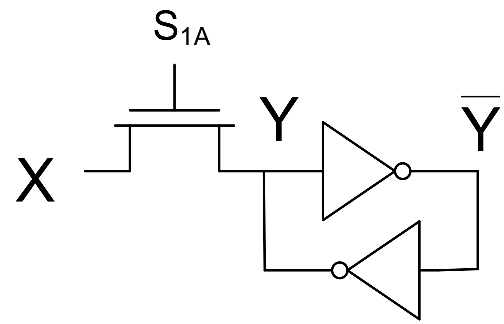
Standard 6-transistor SRAM Cell

The two-inverter loop



S_{1B} can also be eliminated (opened)

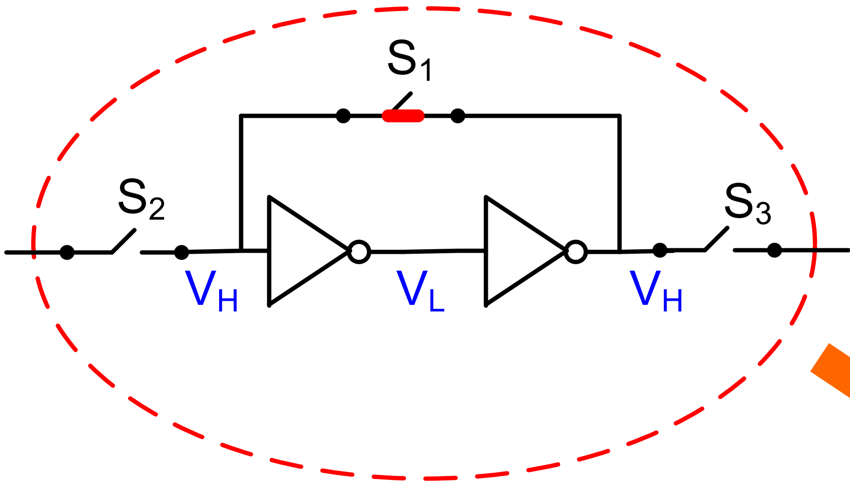
S_2 often eliminated (shorted)

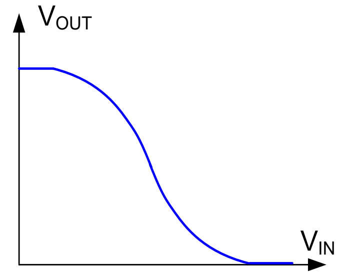


5-transistor SRAM Cell

Will also work but less common (less area but degraded performance)

Ask the inverter how it will interpret logic levels

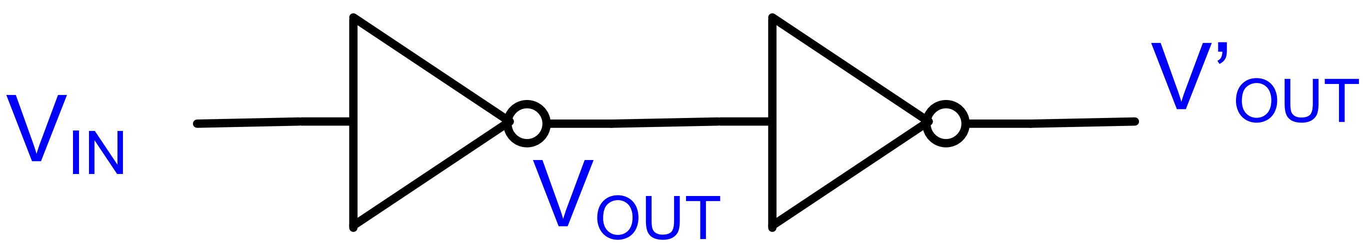




Inverter Characteristics

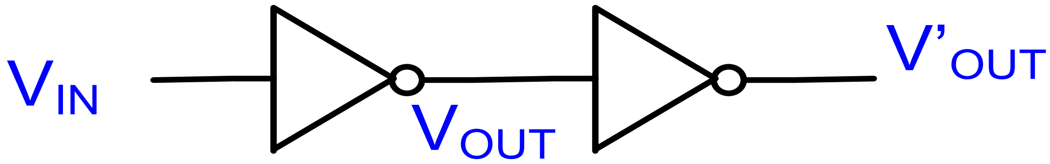
V_H=?

V_L=?

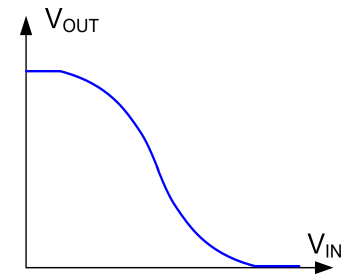


Thus, consider the inverter pair

Ask the inverter how it will interpret logic levels



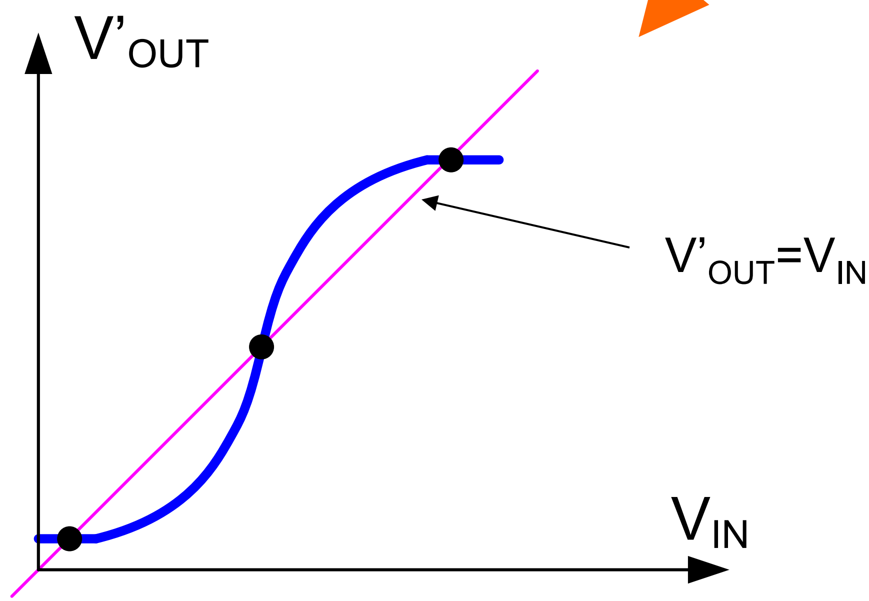
Inverter pair



V_H=?

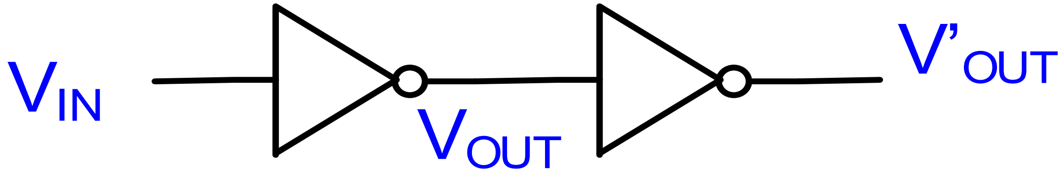
V_L=?

V_H and V_L will be on the intersection of the transfer characteristics of the inverter pair (IPTC) and the $V'_{OUT}=V_{IN}$ line

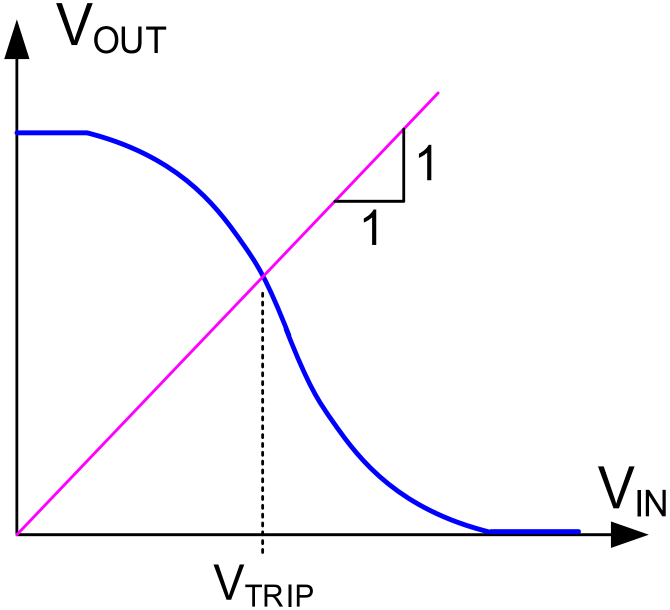


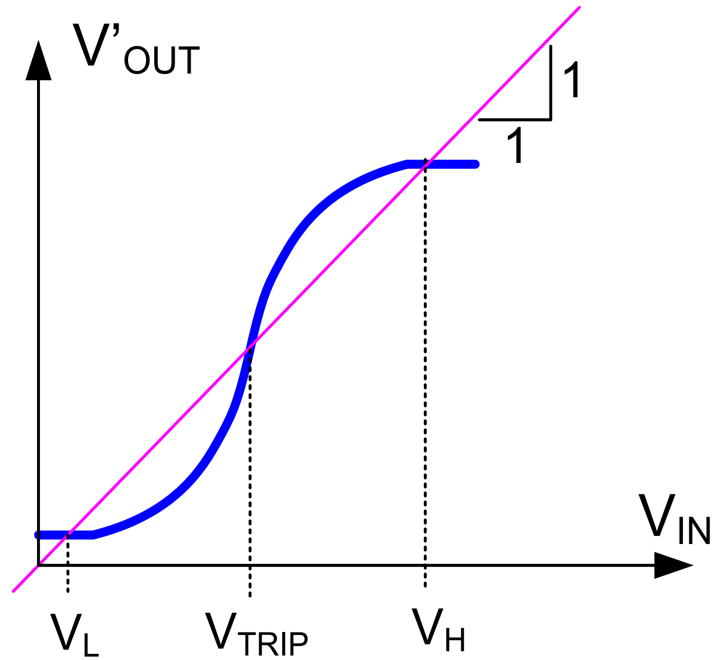
V_H and V_L often termed the “1” and “0” states

Observation



When V_{OUT}=V_{IN} for the inverter, V'_{OUT} is also equal to V_{IN}. Thus the intersection point for V_{OUT}=V_{IN} in the inverter transfer characteristics (ITC) is also an intersection point for V'_{OUT}=V_{IN} in the inverter-pair transfer characteristics (IPTC). This intersection point is defined as V_{TRIP}





Implication: Inverter characteristics can be used directly to obtain V_{TRIP}

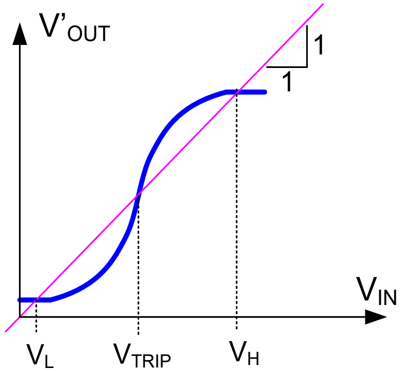
Logic Family Characteristics

What properties of an inverter are necessary for it to be useful for building a two-level logic family?

The inverter-pair transfer characteristics must have three unique intersection points with the $V'_{OUT} = V_{IN}$ line

What are the logic levels for a given inverter of for a given logic family?

The two extreme intersection points of the inverter-pair transfer characteristics with the $V'_{OUT} = V_{IN}$ line



Can we legislate V_H and V_L for a logic family ? No!

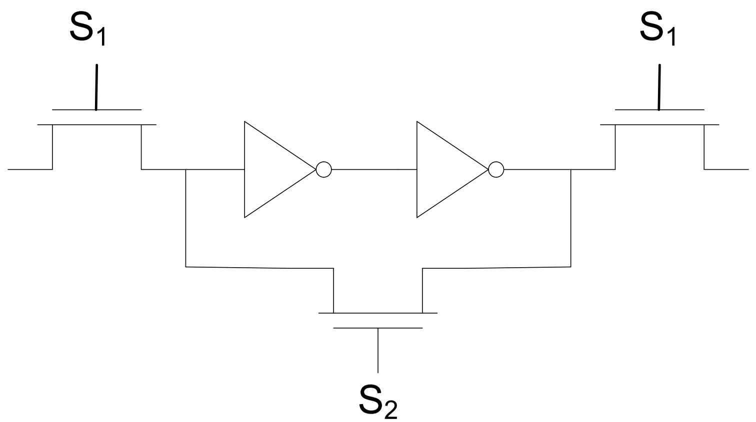
What other properties of the inverter are desirable?

Reasonable separation between V_H and V_L (enough separation so that noise does not cause circuit to interpret level incorrectly) Often thought to want

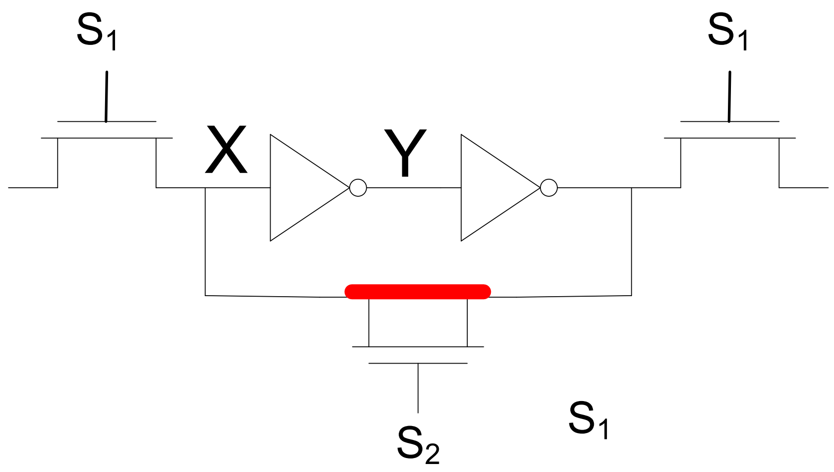
$$V_{TRIP} \cong \frac{V_H + V_L}{2}$$

(to provide adequate noise immunity and process insensitivity)

What happens near the quasi-stable operating point?

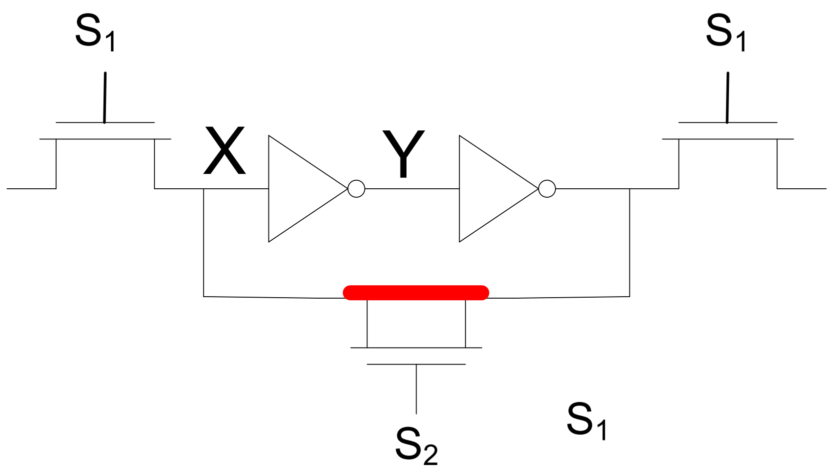


S_2 closed and $X=Y=V_{TRIP}$



What happens near the quasi-stable operating point?

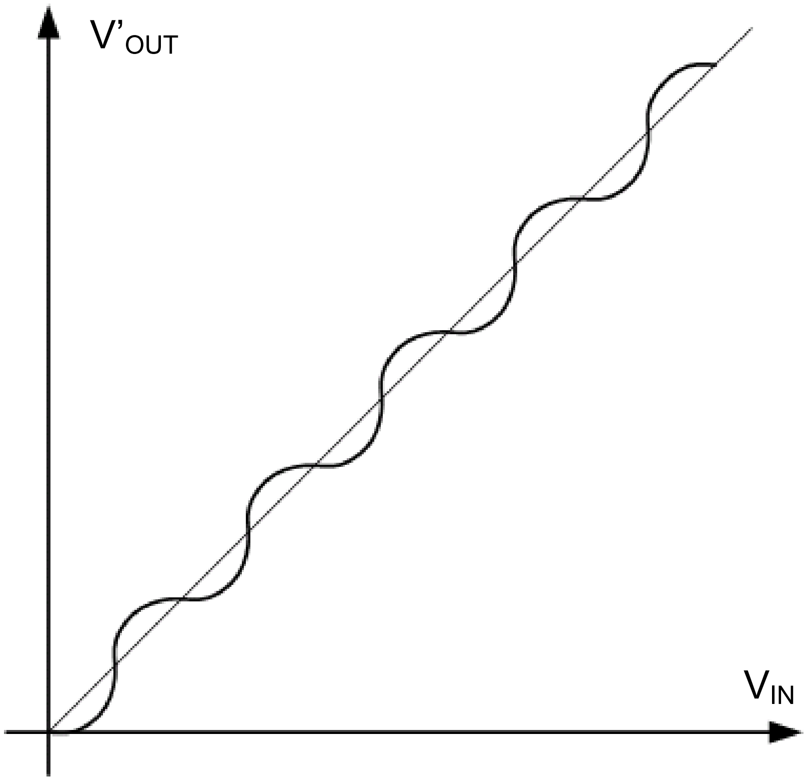
S_2 closed and $X=Y=V_{TRIP}$



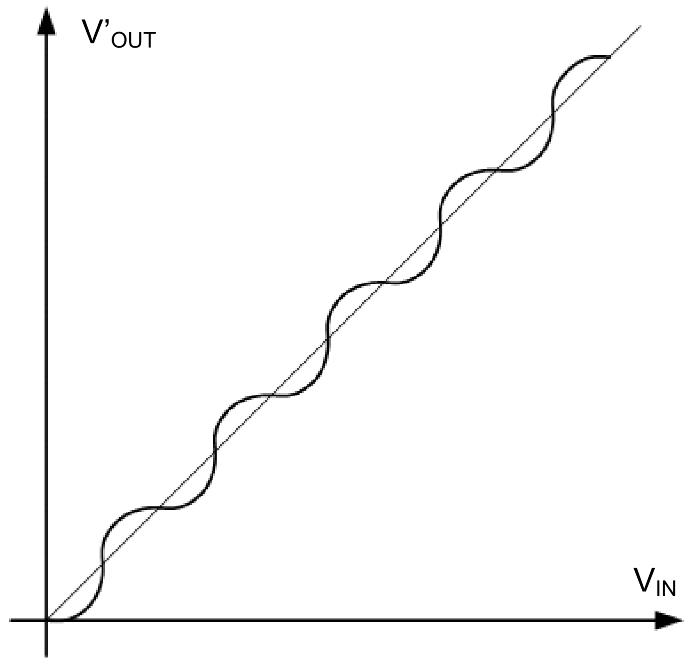
If X decreases even very slightly, will move to the X=0, Y=1 state (very fast)

If X increases even very slightly, will move to the X=1, Y=0 state (very fast)

What if the inverter pair had the following transfer characteristics?

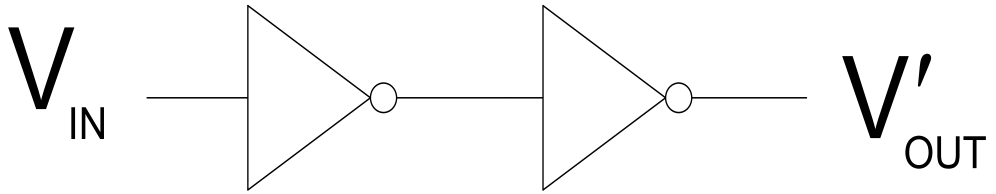


What if the inverter pair had the following transfer characteristics?

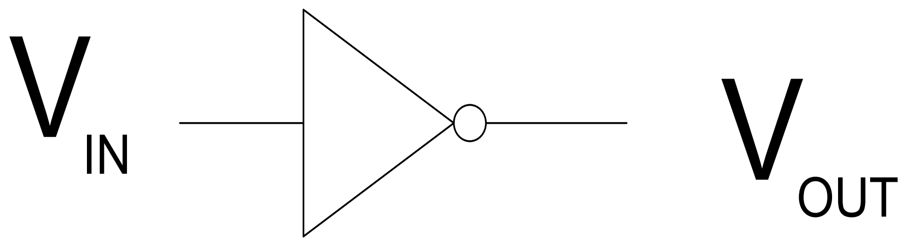


Multiple levels of logic
Every intersection point with slope <1 is a stable point
Every intersection point with slope >1 is a quasi-stable point

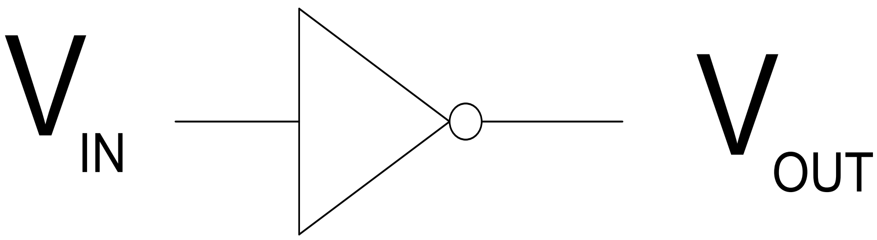
What are the transfer characteristics of the static CMOS inverter pair?

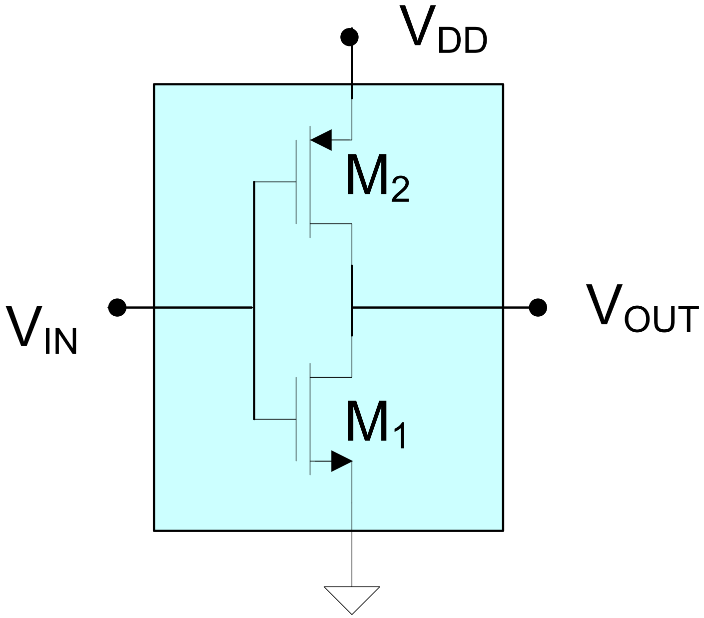


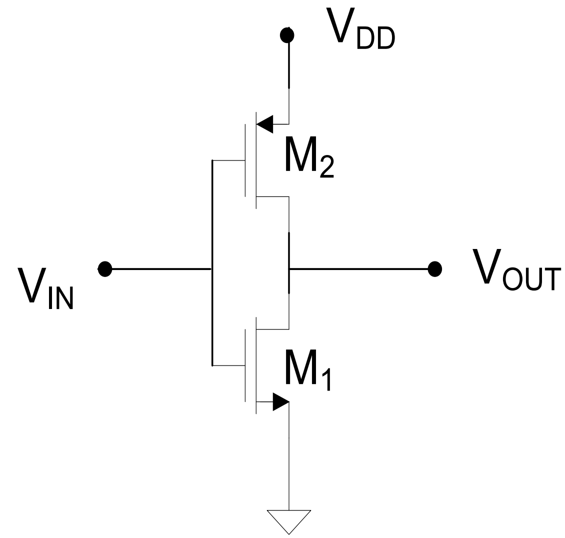
Consider first the inverter



Transfer characteristics of the static CMOS inverter





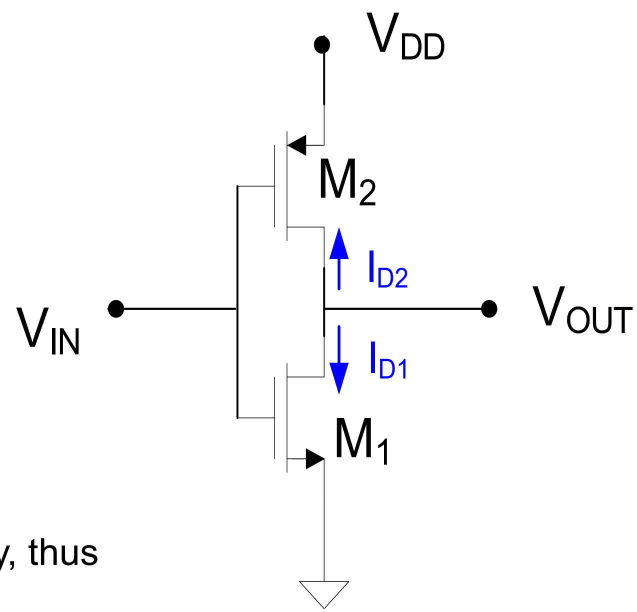


V_{DD}
M_2
V_{IN}
V_{OUT}
M_1

Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

Case 1 Vin is so high that M_1 triode, M_2 cutoff



$$I_{D1} = \mu_n C_{OXn} \frac{W_1}{L_1}\left(V_{IN} - V_{Tn} - \frac{V_{OUT}}{2}\right)V_{OUT}$$

$$I_{D2} = 0$$

Equating I_{D1} and $-I_{D2}$ we obtain:

$$0 = \mu_n C_{OXn} \frac{W_1}{L_1}\left(V_{IN} - V_{Tn} - \frac{V_{OUT}}{2}\right)V_{OUT}$$

It can be shown that setting the first product term to 0 will not verify, thus

$$V_{OUT} = 0$$

valid for:

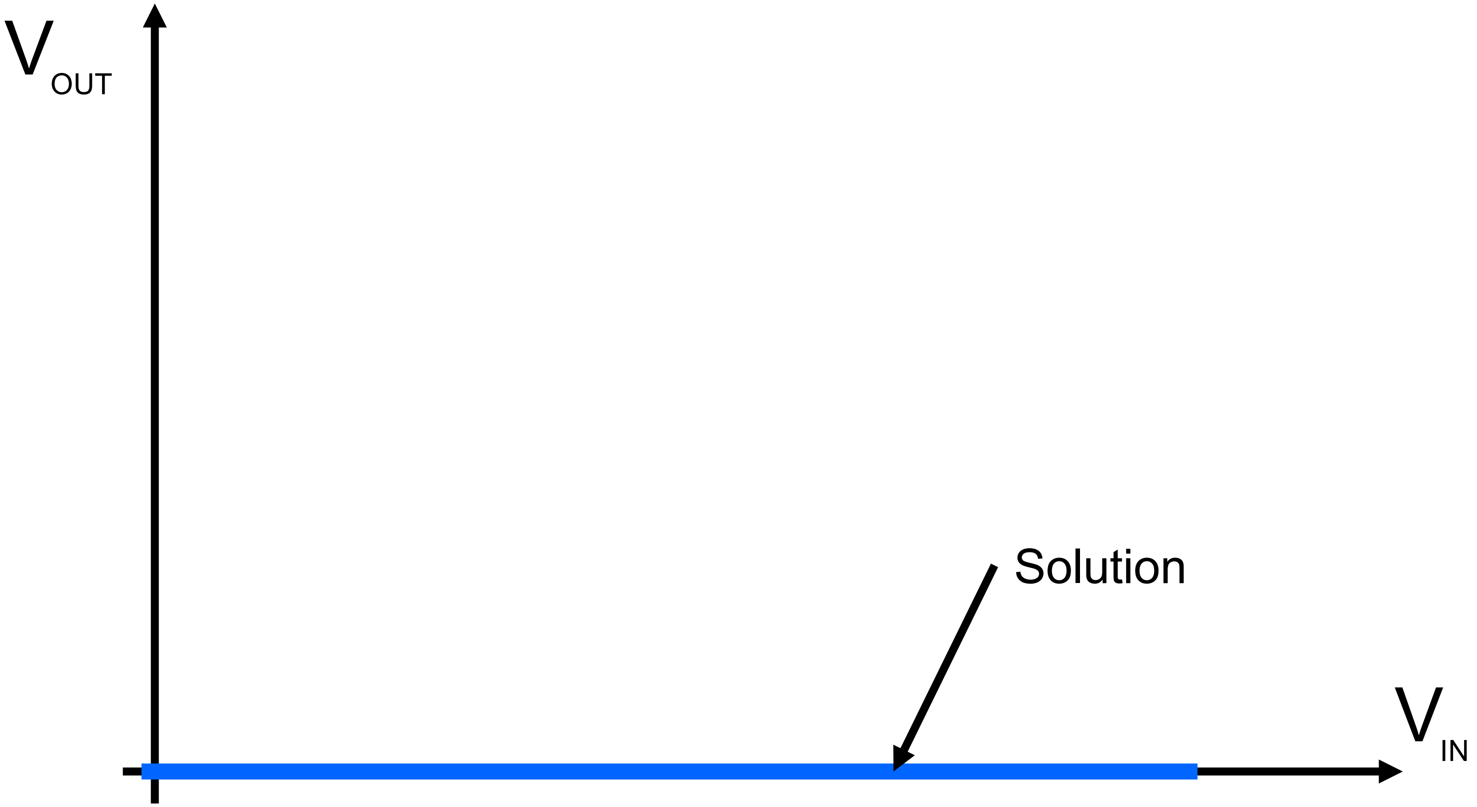
$$V_{GS1} \geq V_{Tn} \qquad V_{DS1} < V_{GS1} - V_{Tn} \qquad V_{GS2} \geq V_{Tp}$$

thus, valid for:

$$V_{IN} \geq V_{Tn} \qquad V_{OUT} < V_{IN} - V_{Tn} \qquad V_{IN} - V_{DD} \geq V_{Tp}$$

Graphical Interpretation of these conditions:

$$V_{IN} \geq V_{Tn} \qquad V_{OUT} < V_{IN} - V_{Tn} \qquad V_{IN} - V_{DD} \geq V_{Tp}$$

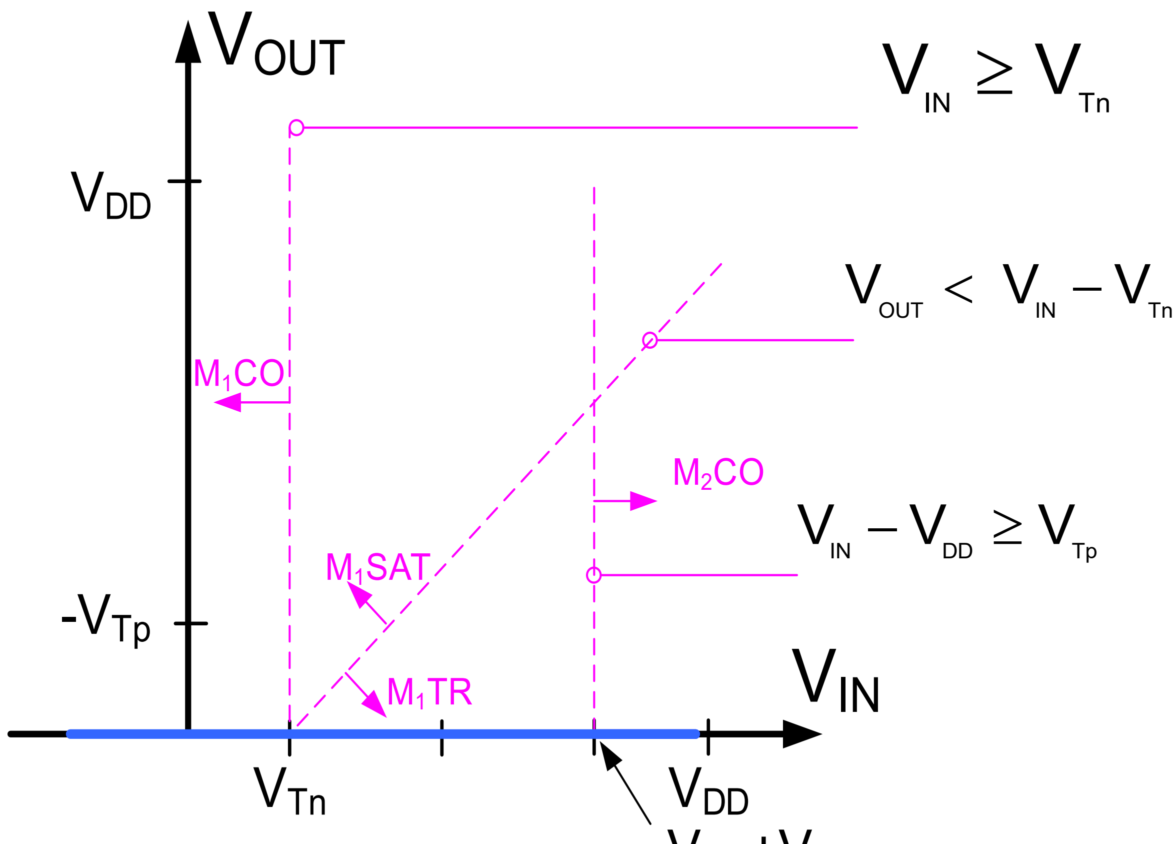


Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

Case 1 M_1 triode, M_2 cutoff

$$V_{OUT} = 0$$

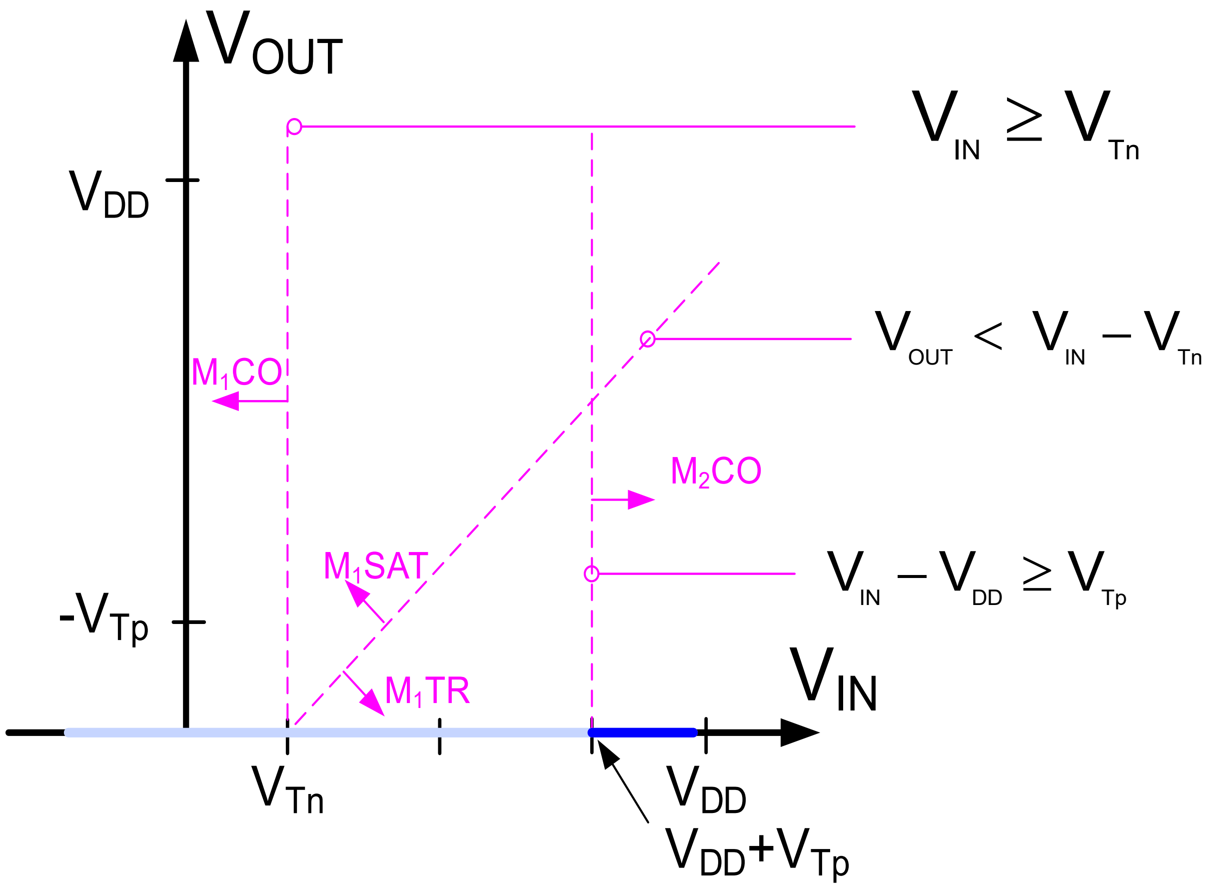


Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

Case 1 M_1 triode, M_2 cutoff

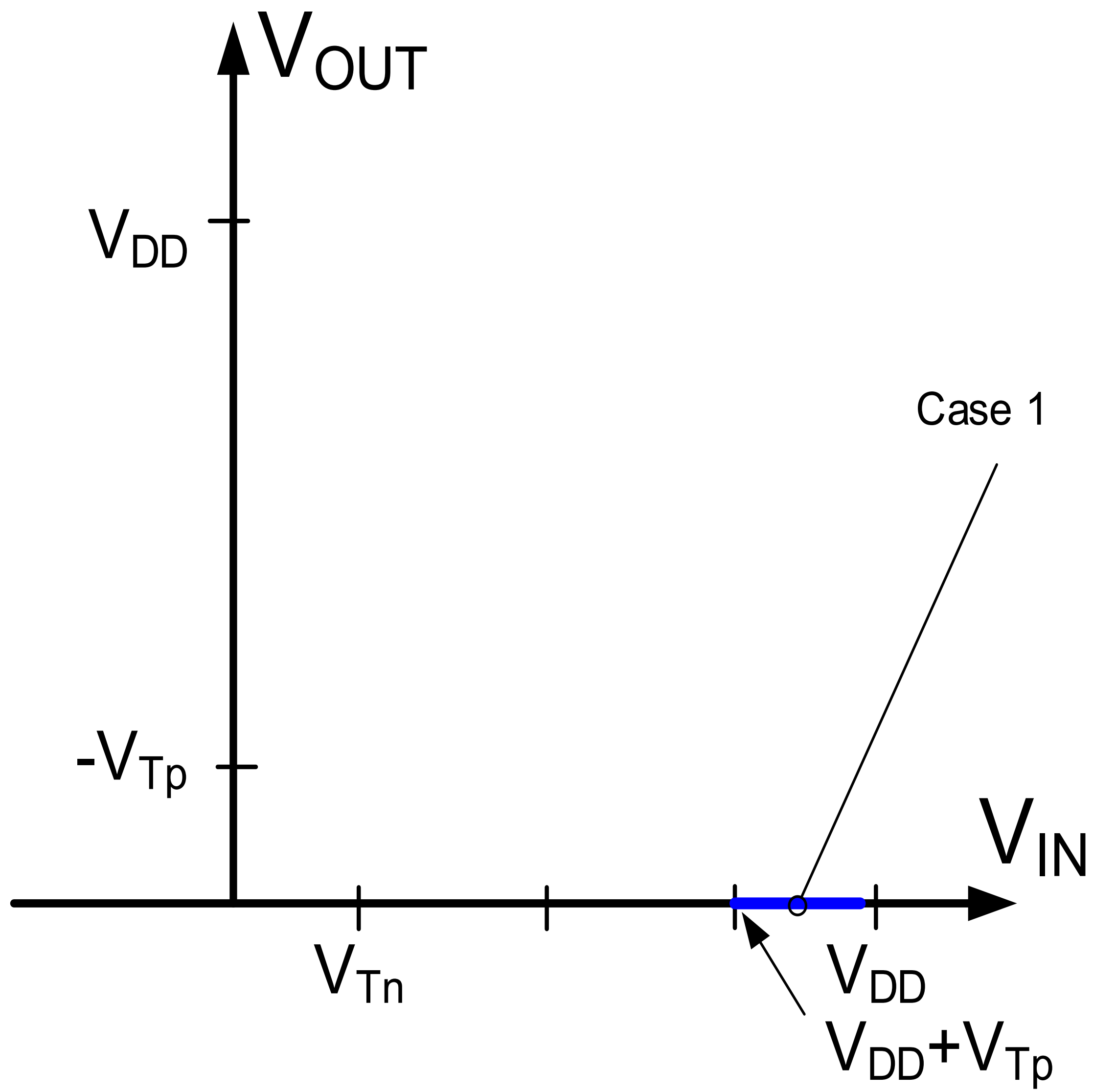
$$V_{OUT} = 0$$



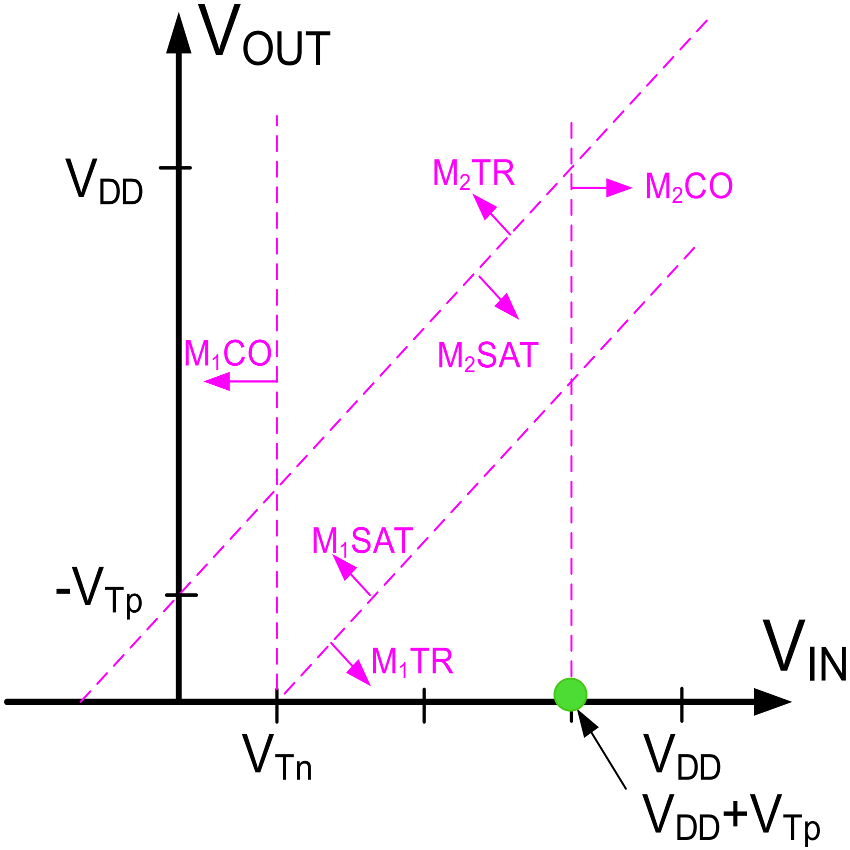
Transfer characteristics of the static CMOS inverter

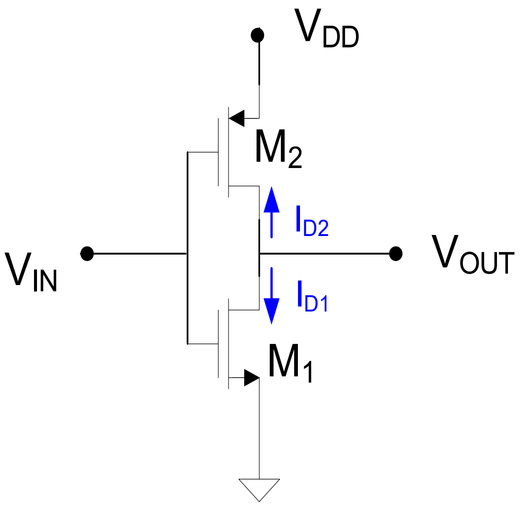
(Neglect λ effects)

Partial solution:



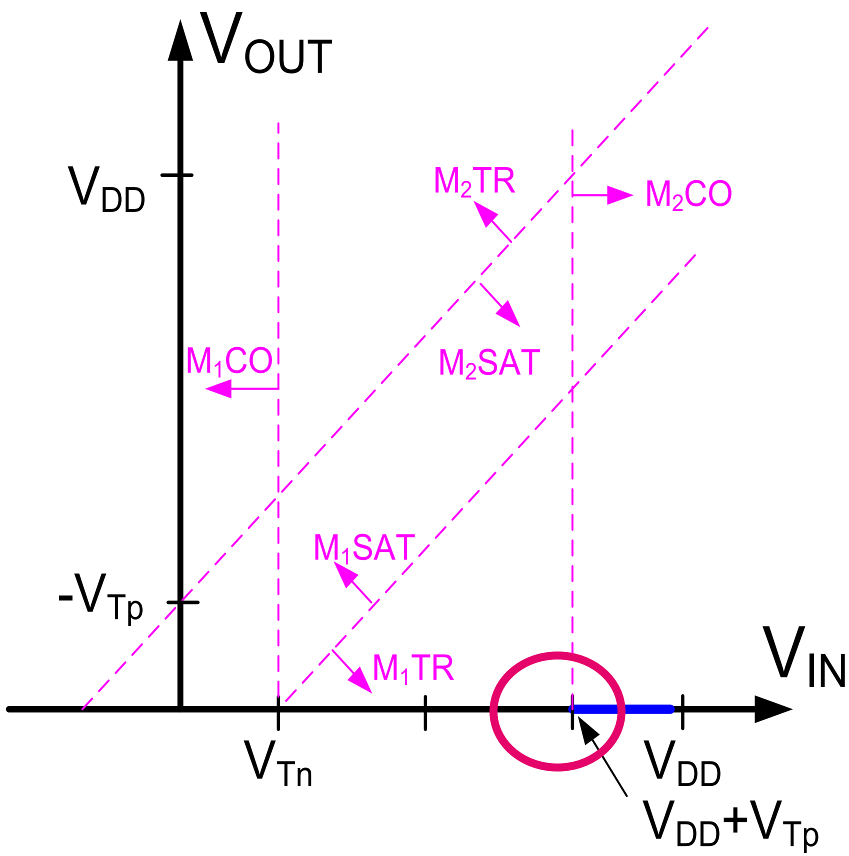
Regions of Operation for Devices in CMOS inverter





Transfer characteristics of the static CMOS inverter
(Neglect λ effects)

Case 2 M_1 triode, M_2 sat

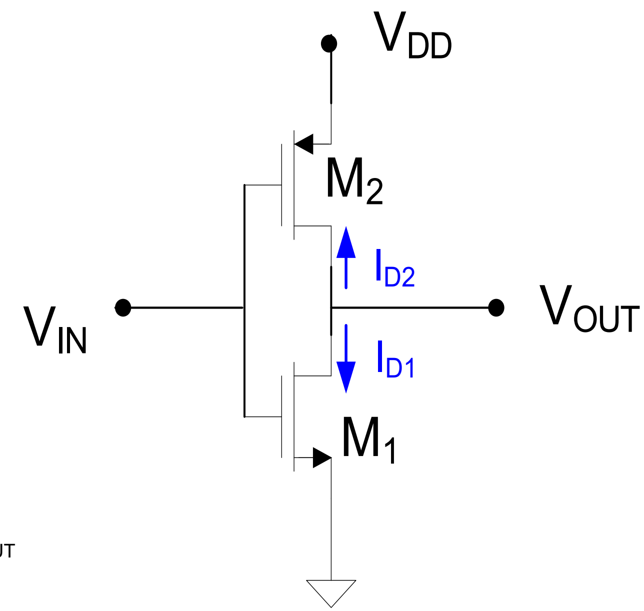


M_2: Square law I_D

M_1: like a resistor

Transfer characteristics of the static CMOS inverter

(Neglect λ effects)



Case 2 M_1 triode, M_2 sat

$$I_{D1} = \mu_n C_{OXn} \frac{W_1}{L_1}\left(V_{IN} - V_{Tn} - \frac{V_{OUT}}{2}\right)V_{OUT}$$

$$I_{D2} = -\frac{\mu_p C_{OXp}}{2}\frac{W_2}{L_2}\left(V_{IN} - V_{DD} - V_{Tp}\right)^2$$

Equating I_{D1} and $-I_{D2}$ we obtain:

$$\frac{\mu_p C_{OXp}}{2}\frac{W_2}{L_2}\left(V_{IN} - V_{DD} - V_{Tp}\right)^2 = \mu_n C_{OXn} \frac{W_1}{L_1}\left(V_{IN} - V_{Tn} - \frac{V_{OUT}}{2}\right)V_{OUT}$$

valid for:

$$V_{GS1} \geq V_{Tn} \qquad V_{DS1} < V_{GS1} - V_{Tn} \qquad V_{GS2} \leq V_{Tp} \qquad V_{DS2} \leq V_{GS2} - V_{T2}$$

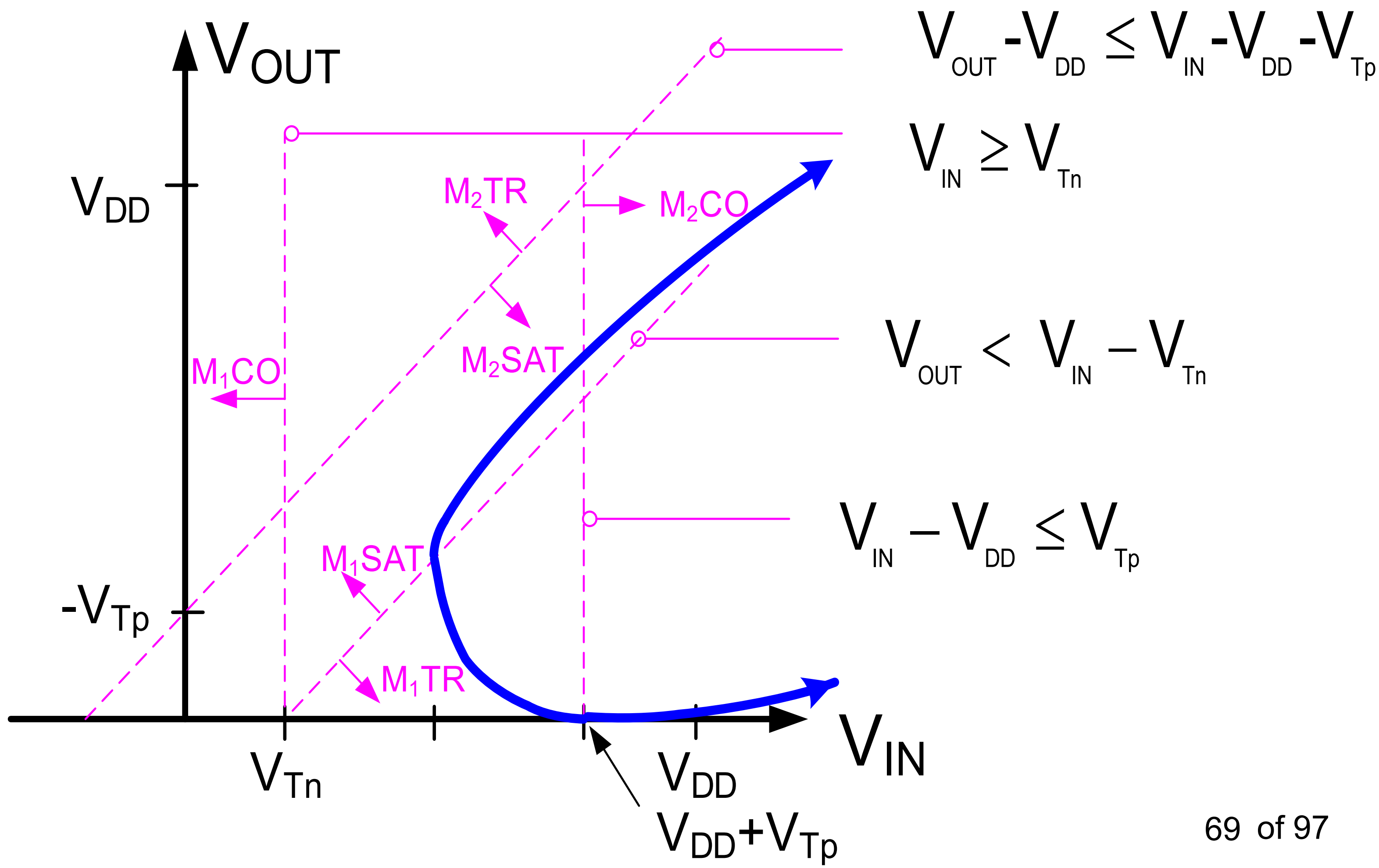
thus, valid for:

$$V_{IN} \geq V_{Tn} \qquad V_{OUT} < V_{IN} - V_{Tn} \qquad V_{IN} - V_{DD} \leq V_{Tp} \qquad V_{OUT} - V_{DD} \leq V_{IN} - V_{DD} - V_{Tp}$$

Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

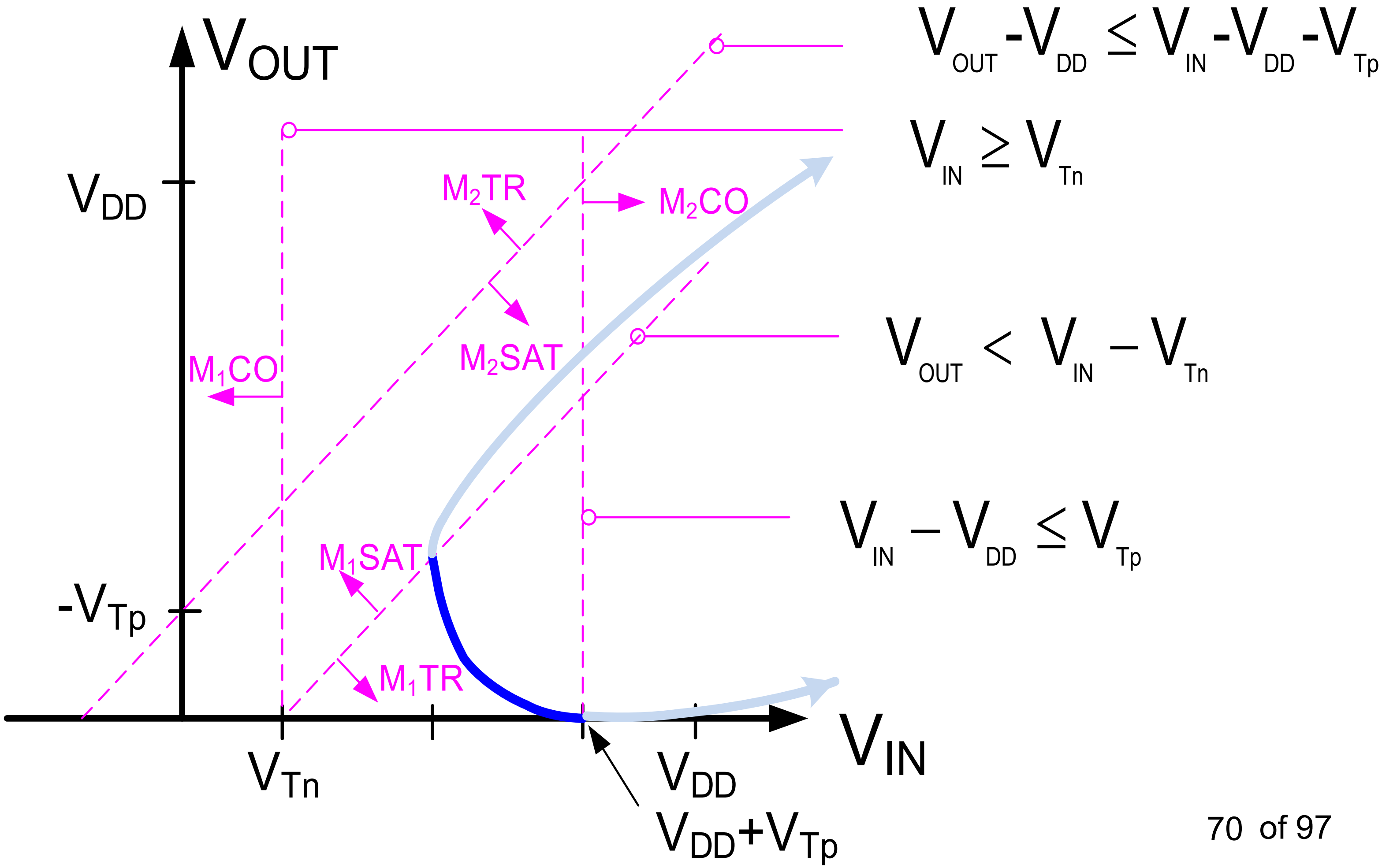
Case 2 M_1 triode, M_2 sat



Transfer characteristics of the static CMOS inverter

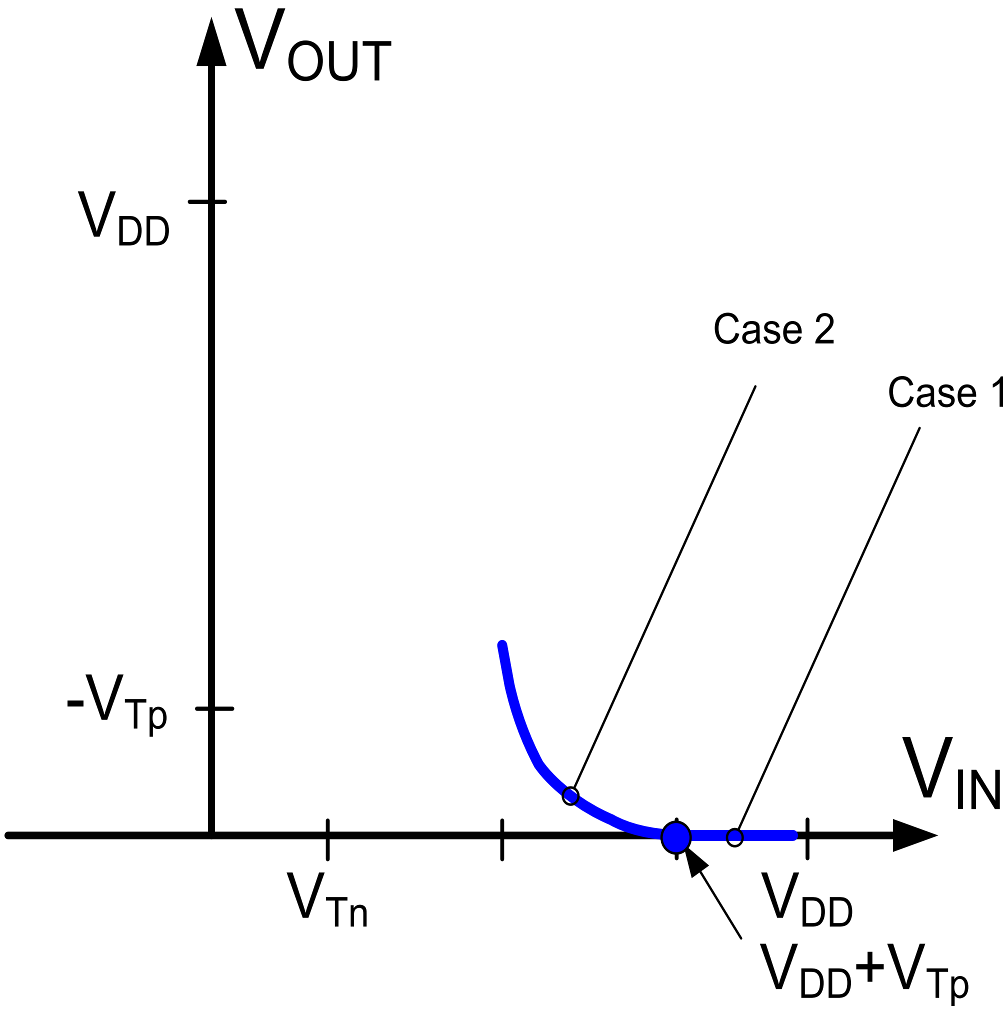
(Neglect λ effects)

Case 2 M_1 triode, M_2 sat



Transfer characteristics of the static CMOS inverter

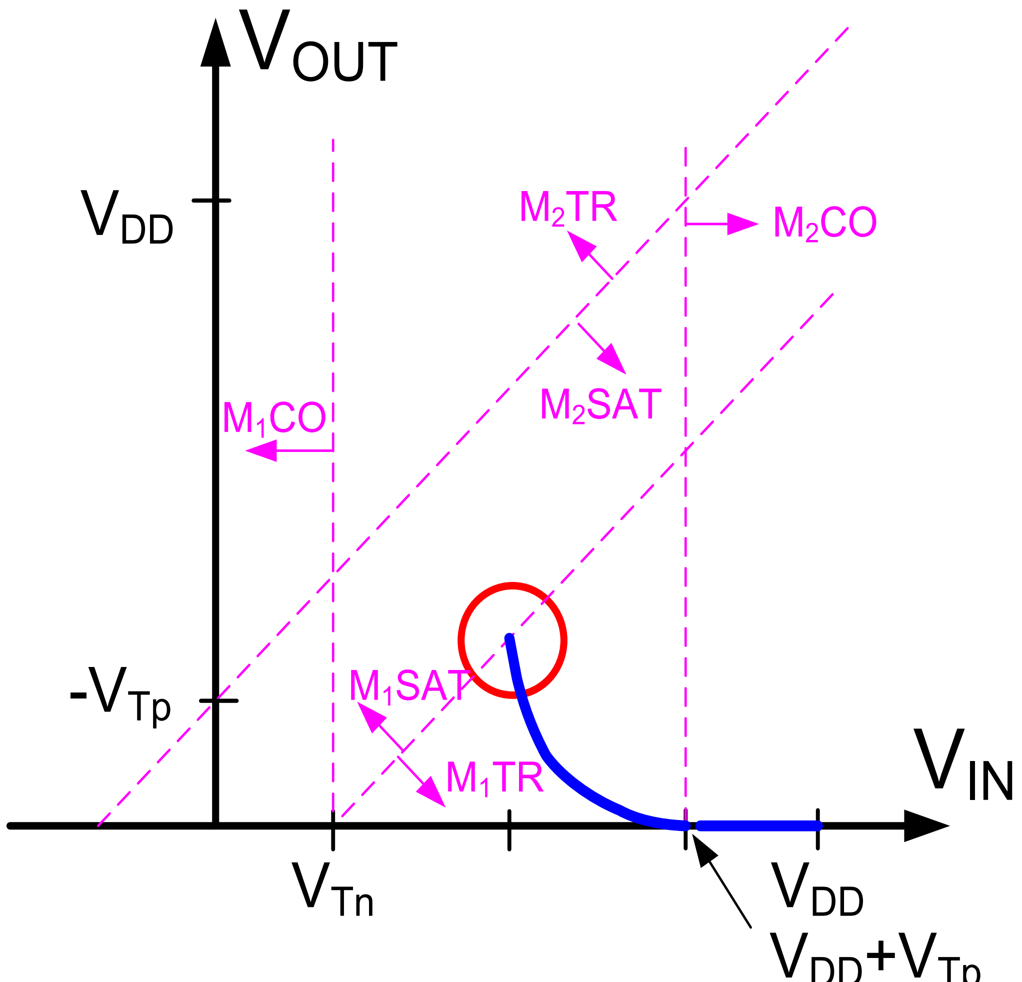
Partial solution:



Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

Case 3 M_1 sat, M_2 sat



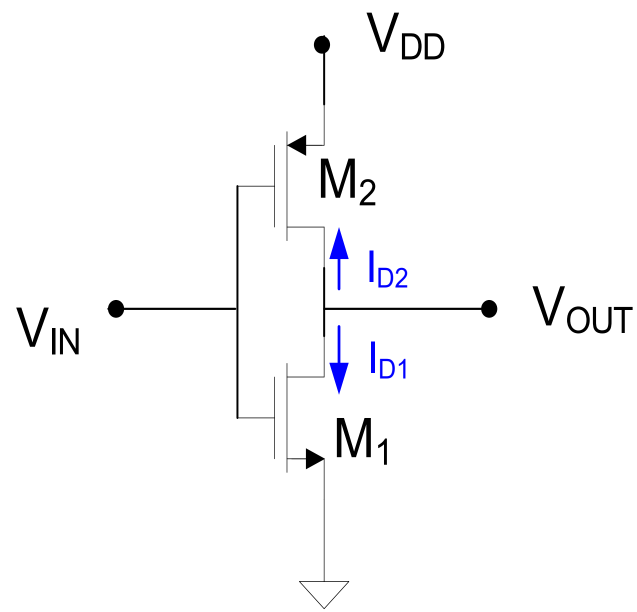
Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

Case 3 M_1 sat, M_2 sat

$$I_{D1} = \frac{\mu_n C_{OXn}}{2}\frac{W_1}{L_1}\left(V_{IN} - V_{Tn}\right)^2$$

$$I_{D2} = \frac{\mu_p C_{OXp}}{2}\frac{W_2}{L_2}\left(V_{IN} - V_{DD} - V_{Tp}\right)^2$$



Equating I_{D1} and $-I_{D2}$ we obtain:

$$\frac{\mu_p C_{OXp}}{2}\frac{W_2}{L_2}\left(V_{IN} - V_{DD} - V_{Tp}\right)^2 = \frac{\mu_n C_{OXn}}{2}\frac{W_1}{L_1}\left(V_{IN} - V_{Tn}\right)^2$$

Which can be rewritten as:

$$\sqrt{\frac{\mu_p C_{OXp}}{2}\frac{W_2}{L_2}}\left(V_{DD} + V_{Tp} - V_{IN}\right) = \sqrt{\frac{\mu_n C_{OXn}}{2}\frac{W_1}{L_1}}\left(V_{IN} - V_{Tn}\right)$$

Which can be simplified to:

$$V_{IN} = \frac{\left(V_{Tn}\right)\sqrt{\frac{\mu_n C_{OXn}}{2}\frac{W_1}{L_1}} + \left(V_{DD} + V_{Tp}\right)\sqrt{\frac{\mu_p C_{OXp}}{2}\frac{W_2}{L_2}}}{\sqrt{\frac{\mu_n C_{OXn}}{2}\frac{W_1}{L_1}} + \sqrt{\frac{\mu_p C_{OXp}}{2}\frac{W_2}{L_2}}}$$

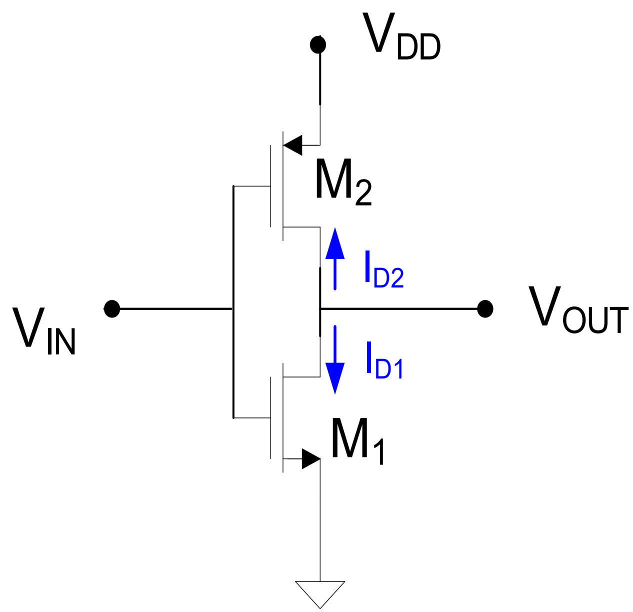
This is a vertical line

Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

Case 3 M_1 sat, M_2 sat

$$V_{IN}=\frac{(V_{Tn})\sqrt{\frac{\mu_nC_{OXn}}{2}\frac{W_1}{L_1}}+(V_{DD}+V_{Tp})\sqrt{\frac{\mu_pC_{OXp}}{2}\frac{W_2}{L_2}}}{\sqrt{\frac{\mu_nC_{OXn}}{2}\frac{W_1}{L_1}}+\sqrt{\frac{\mu_pC_{OXp}}{2}\frac{W_2}{L_2}}}$$



Since $C_{OXn}\cong C_{OXp}=C_{OX}$ this can be simplified to:

$$V_{IN}=\frac{(V_{Tn})\sqrt{\frac{W_1}{L_1}}+(V_{DD}+V_{Tp})\sqrt{\frac{\mu_p}{\mu_n}\frac{W_2}{L_2}}}{\sqrt{\frac{W_1}{L_1}}+\sqrt{\frac{\mu_p}{\mu_n}\frac{W_2}{L_2}}}$$

valid for:

$$V_{GS1}\geq V_{Tn} \qquad V_{DS1}\geq V_{GS1}-V_{Tn} \qquad V_{GS2}\leq V_{Tp} \qquad V_{DS2}\leq V_{GS2}-V_{T2}$$

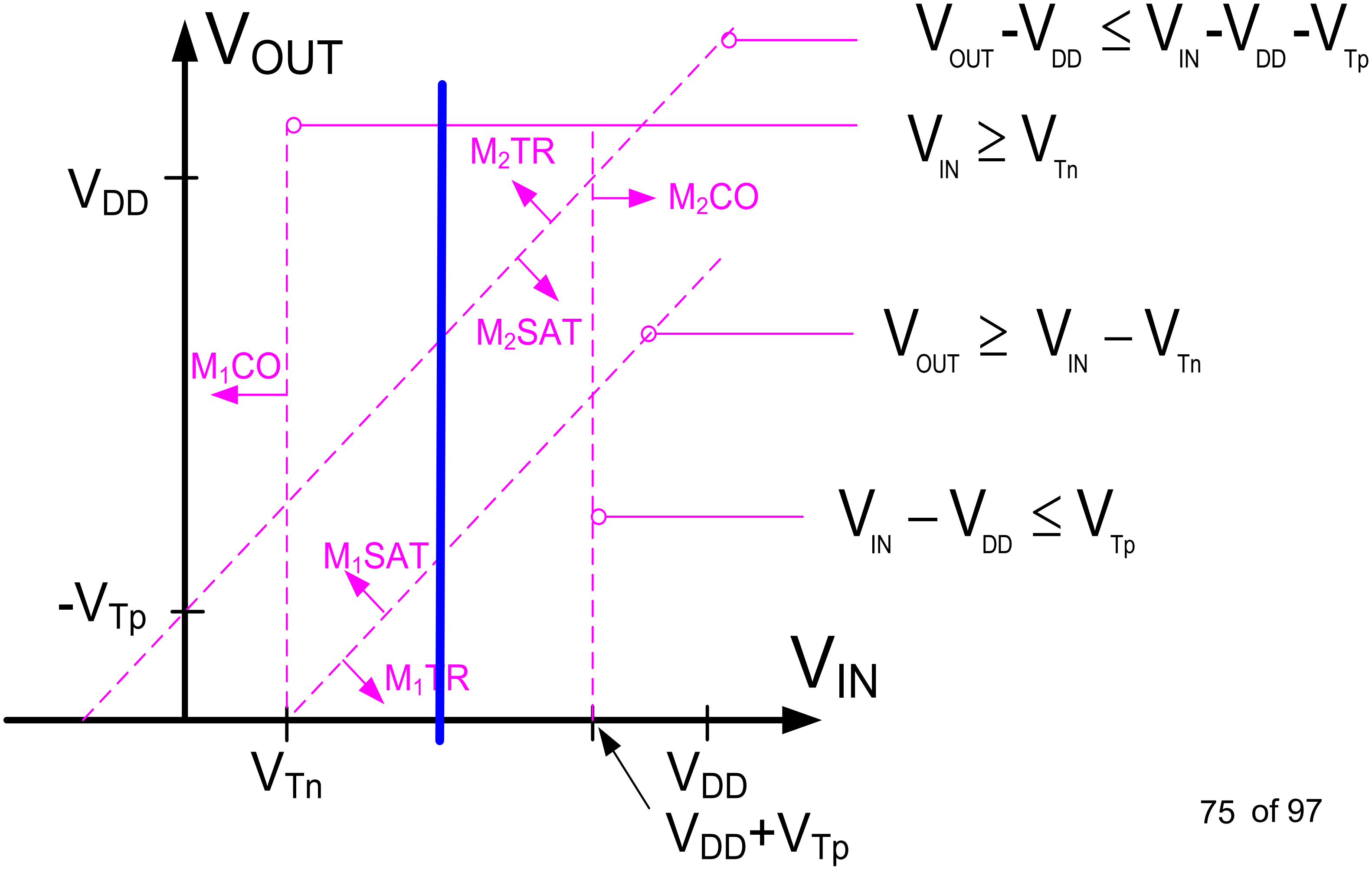
thus, valid for:

$$V_{IN}\geq V_{Tn} \qquad V_{OUT}\geq V_{IN}-V_{Tn} \qquad V_{IN}-V_{DD}\leq V_{Tp} \qquad V_{OUT}-V_{DD}\leq V_{IN}-V_{DD}-V_{Tp}$$

Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

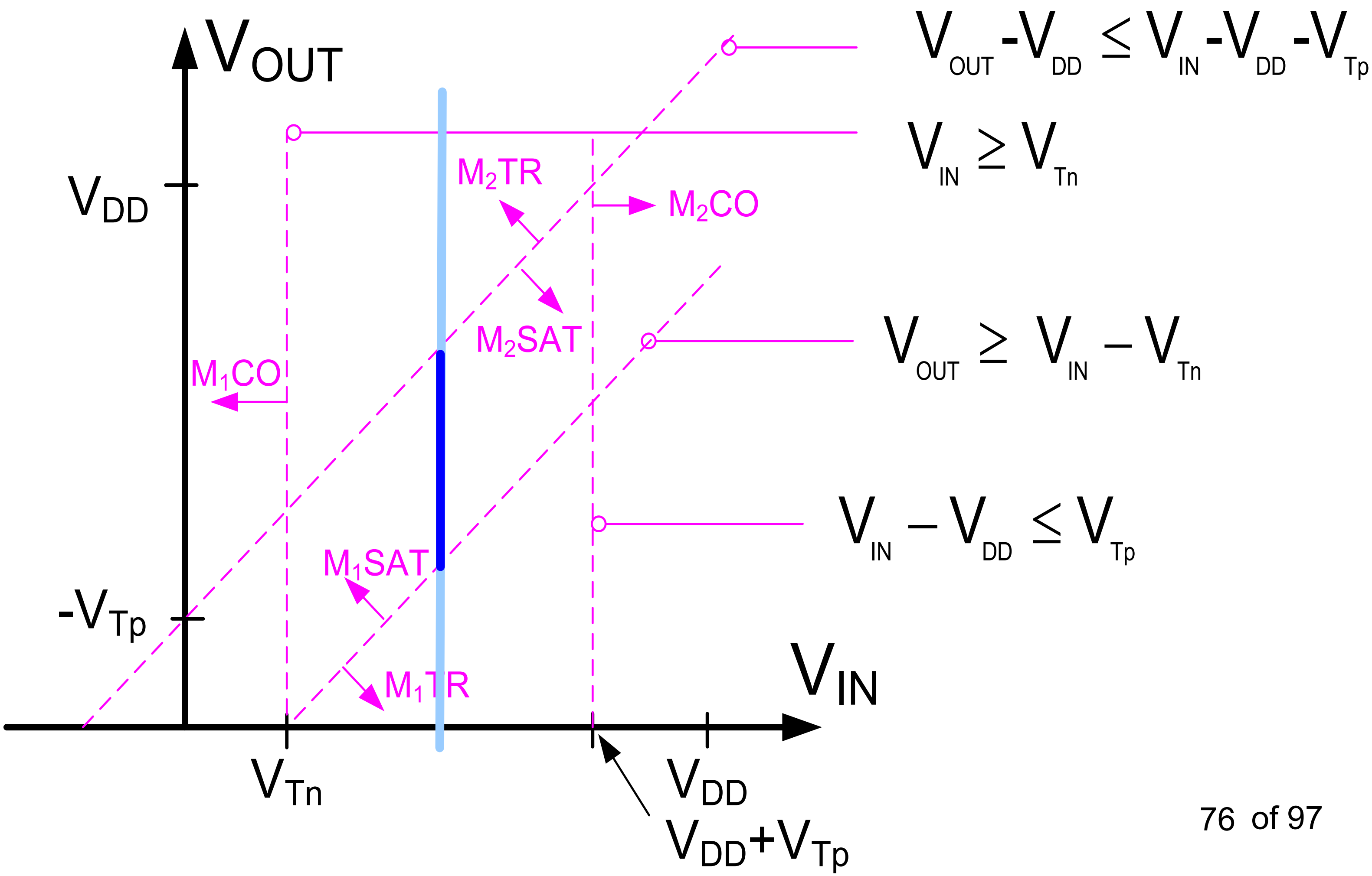
Case 3 M_1 sat, M_2 sat



Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

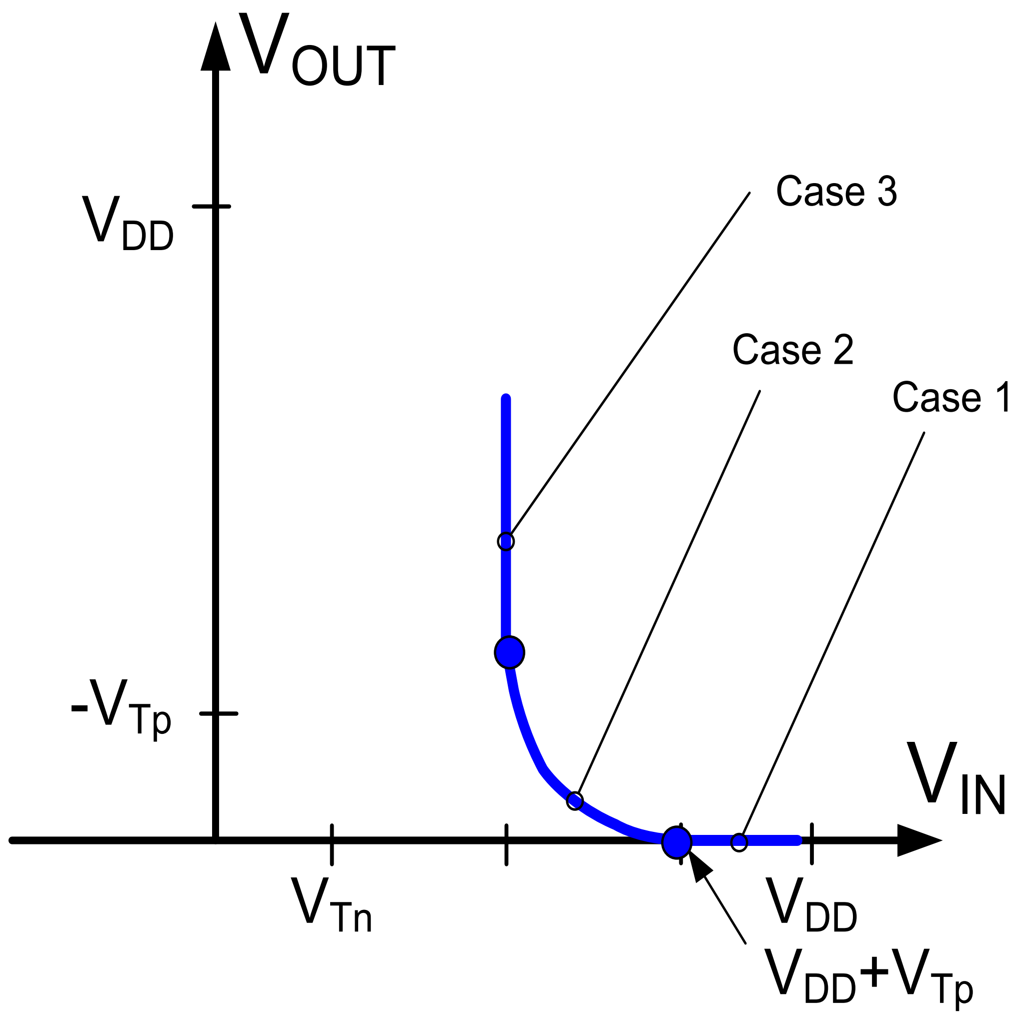
Case 3 M_1 sat, M_2 sat



Transfer characteristics of the static CMOS inverter

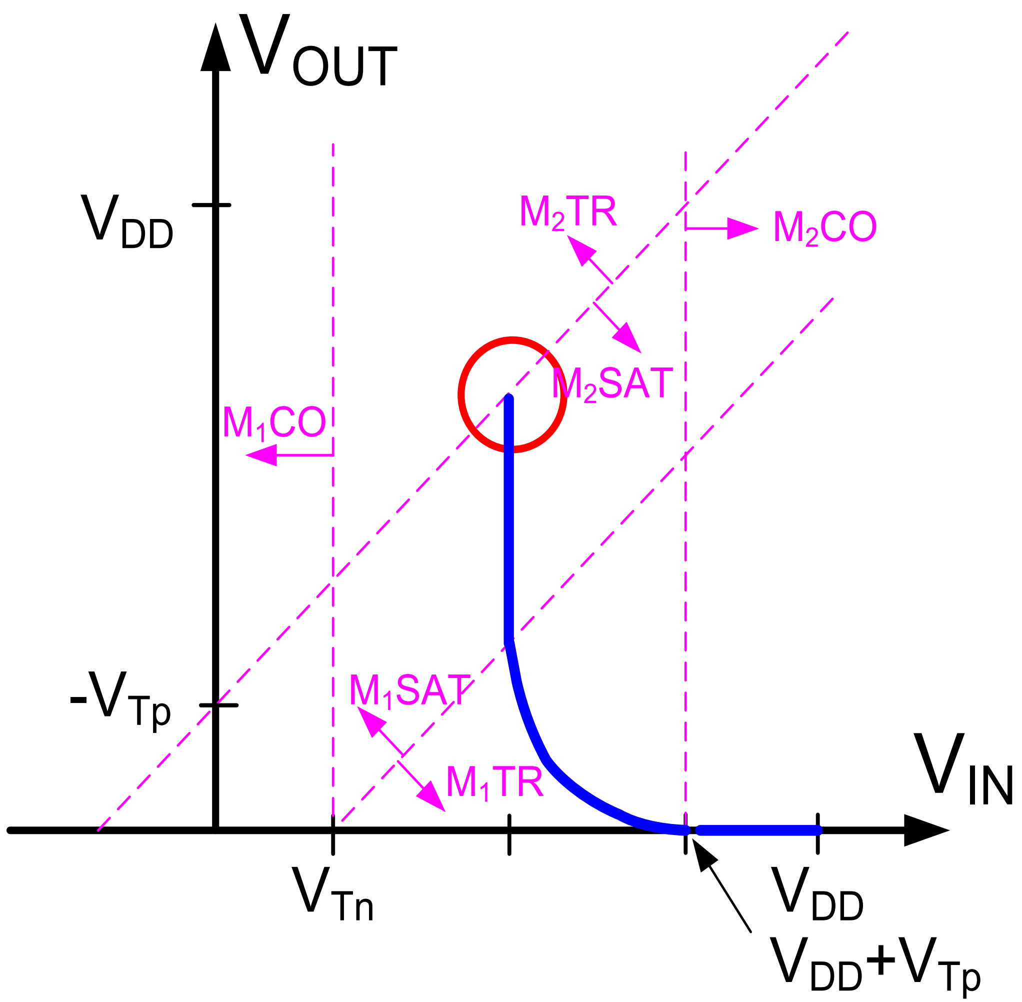
(Neglect λ effects)

Partial solution:



Transfer characteristics of the static CMOS inverter
(Neglect λ effects)

Case 4 M_1 sat, M_2 triode



Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

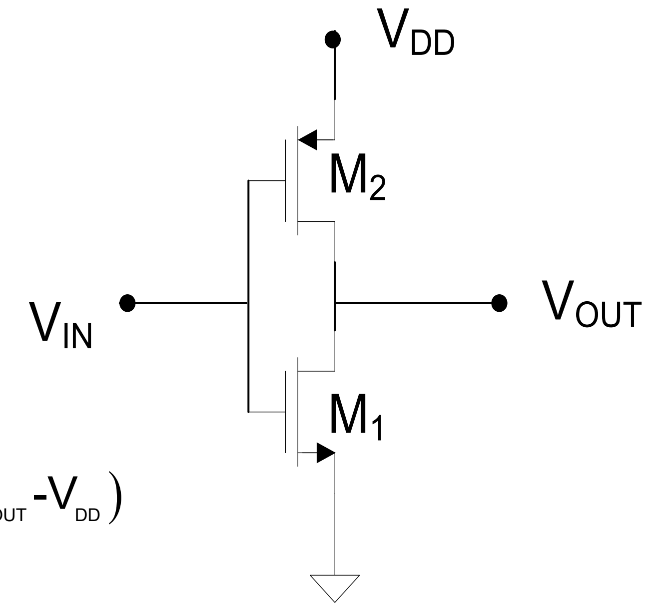
Case 4 M$_1$ sat, M$_2$ triode

$$I_{D1}=\frac{\mu_n C_{OXn}}{2}\frac{W_1}{L_1}\left(V_{IN}-V_{Tn}\right)^2$$

$$I_{D2}=-\mu_p C_{OXp}\frac{W_2}{L_2}\left(V_{IN}-V_{DD}-V_{Tp}-\frac{V_{OUT}\text{-}V_{DD}}{2}\right)\bullet\left(V_{OUT}\text{-}V_{DD}\right)$$

Equating I_{D1} and $-I_{D2}$ we obtain:

$$\frac{\mu_n C_{OXn}}{2}\frac{W_1}{L_1}\left(V_{IN}-V_{Tn}\right)^2=\mu_p C_{OXp}\frac{W_2}{L_2}\left(V_{IN}-V_{DD}-V_{Tp}-\frac{V_{OUT}\text{-}V_{DD}}{2}\right)\bullet\left(V_{OUT}\text{-}V_{DD}\right)$$



valid for:

$$V_{GS1}\geq V_{Tn} \qquad V_{DS1}\geq V_{GS1}-V_{Tn} \qquad V_{GS2}\leq V_{Tp} \qquad V_{DS2}>V_{GS2}\text{-}V_{T2}$$

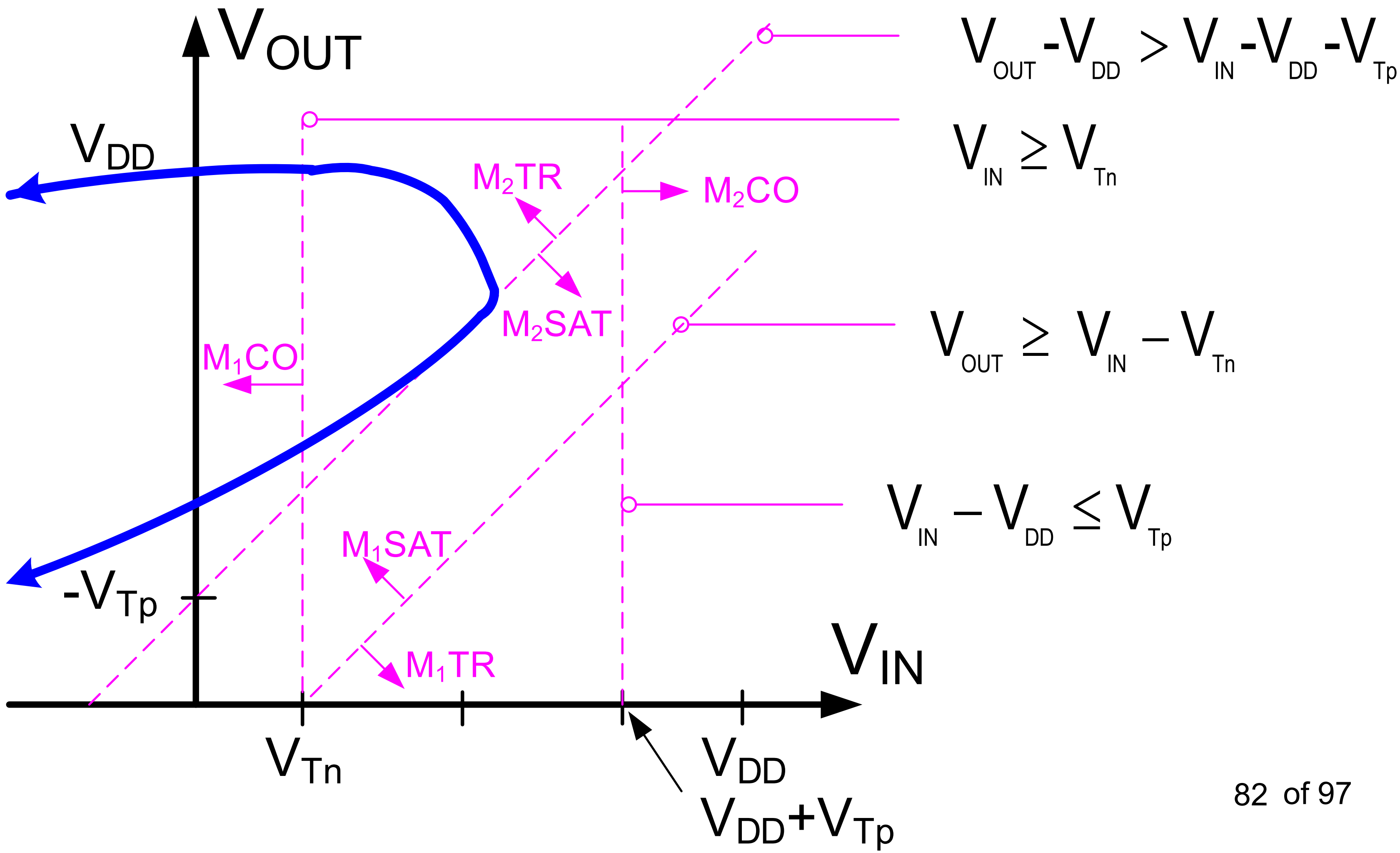
thus, valid for:

$$V_{IN}\geq V_{Tn} \qquad V_{OUT}\geq V_{IN}-V_{Tn} \qquad V_{IN}-V_{DD}\leq V_{Tp} \qquad V_{OUT}\text{-}V_{DD}>V_{IN}\text{-}V_{DD}\text{-}V_{Tp}$$

Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

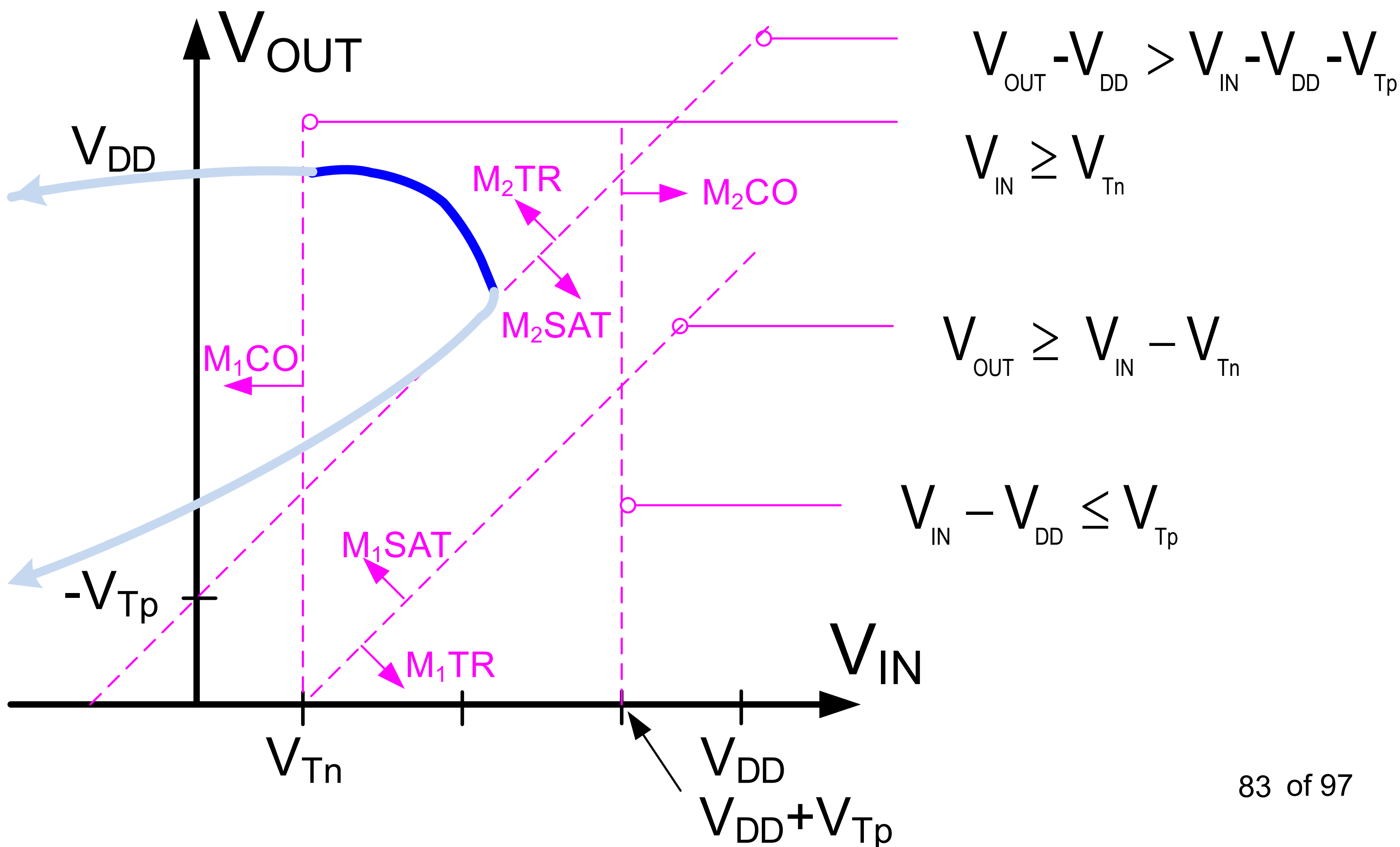
Case 4 M_1 sat, M_2 triode



Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

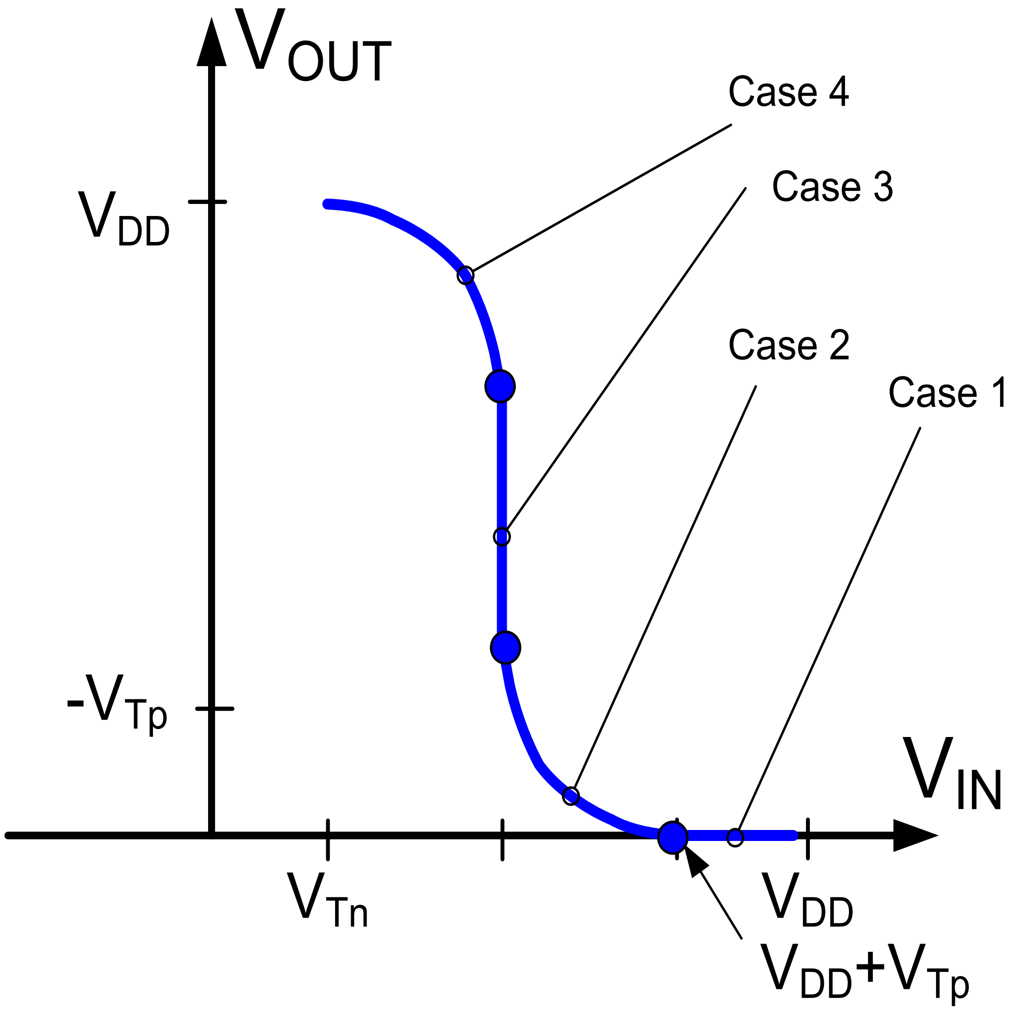
Case 4 M_1 sat, M_2 triode



Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

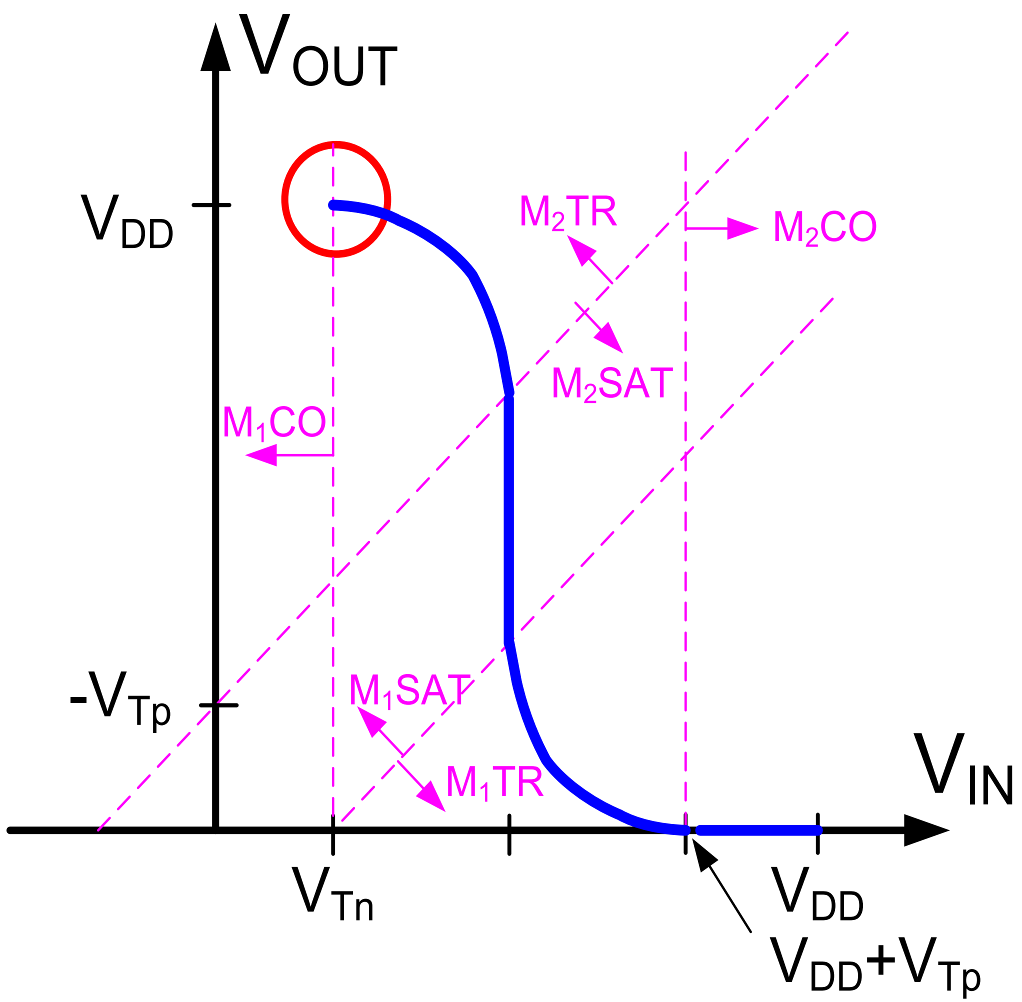
Partial solution:



Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

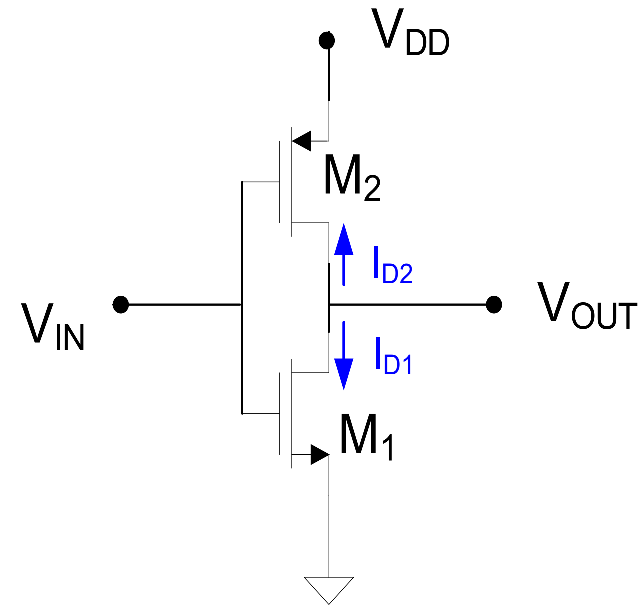
Case 4 M_1 cutoff, M_2 triode



Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

Case 5 M_1 cutoff, M_2 triode



$$I_{D1} = 0$$

$$I_{D2} = -\mu_p C_{OXp} \frac{W_2}{L_2}\left(V_{IN} - V_{DD} - V_{Tp} - \frac{V_{OUT}\text{-}V_{DD}}{2}\right) \bullet \left(V_{OUT}\text{-}V_{DD}\right)$$

Equating I_{D1} and $-I_{D2}$ we obtain:

$$\mu_p C_{OXp} \frac{W_2}{L_2}\left(V_{IN} - V_{DD} - V_{Tp} - \frac{V_{OUT}\text{-}V_{DD}}{2}\right) \bullet \left(V_{OUT}\text{-}V_{DD}\right) = 0$$

valid for:

$$V_{GS1} < V_{Tn} \qquad V_{GS2} \le V_{Tp} \qquad V_{DS2} > V_{GS2}\text{-}V_{T2}$$

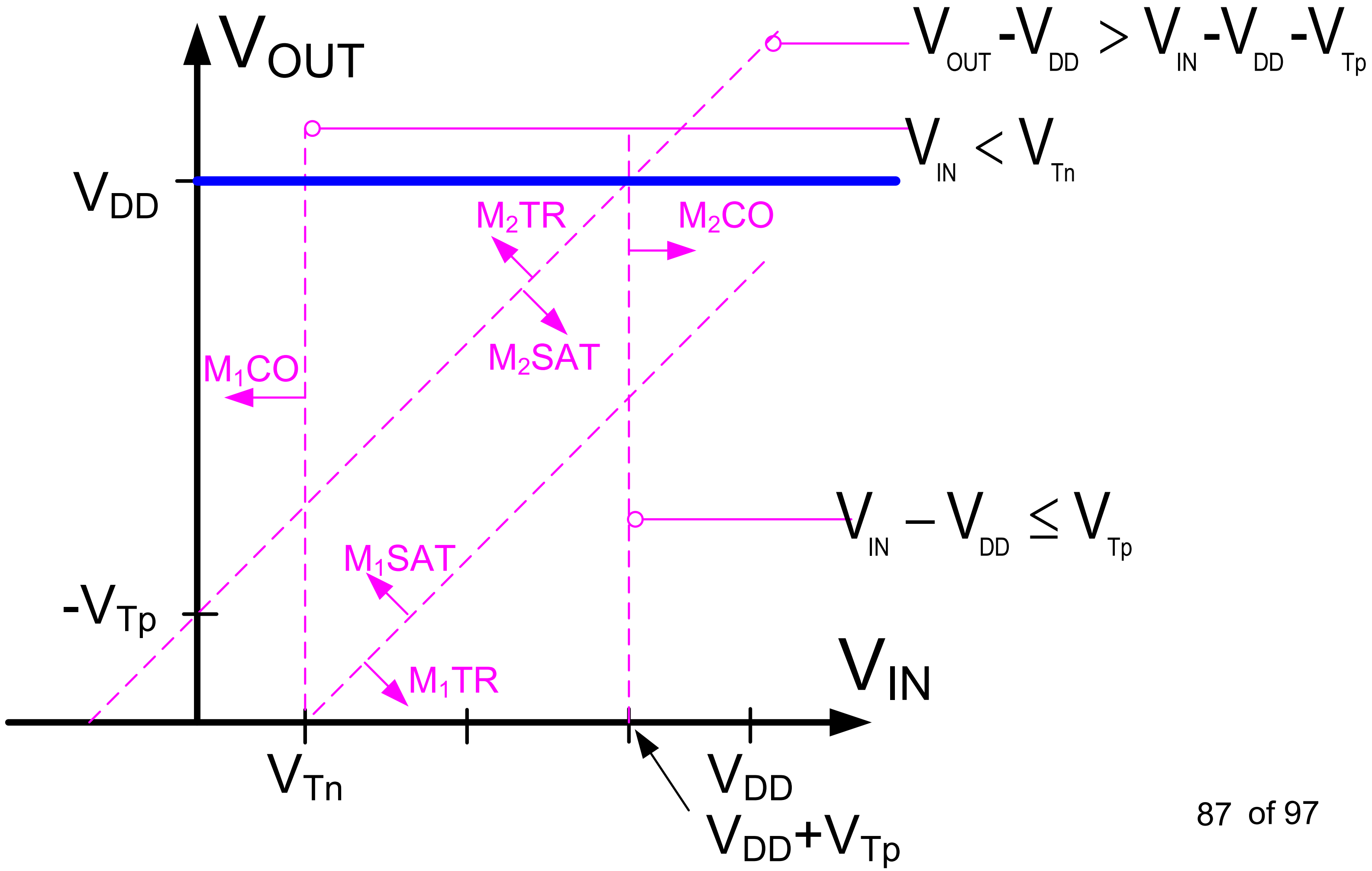
thus, valid for:

$$V_{IN} < V_{Tn} \qquad V_{IN} - V_{DD} \le V_{Tp} \qquad V_{OUT}\text{-}V_{DD} > V_{IN}\text{-}V_{DD}\text{-}V_{Tp}$$

Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

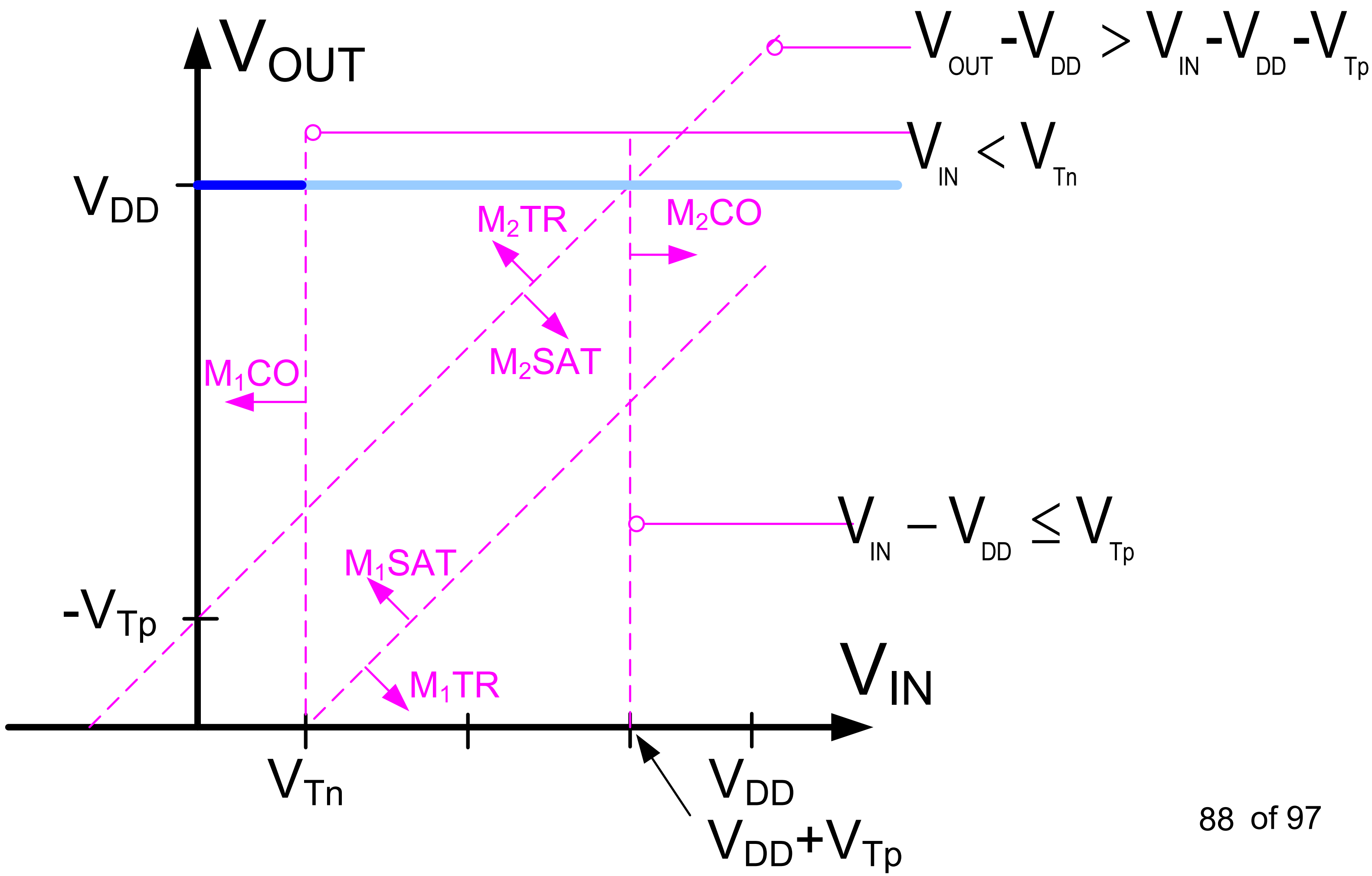
Case 5 M_1 cutoff, M_2 triode



Transfer characteristics of the static CMOS inverter

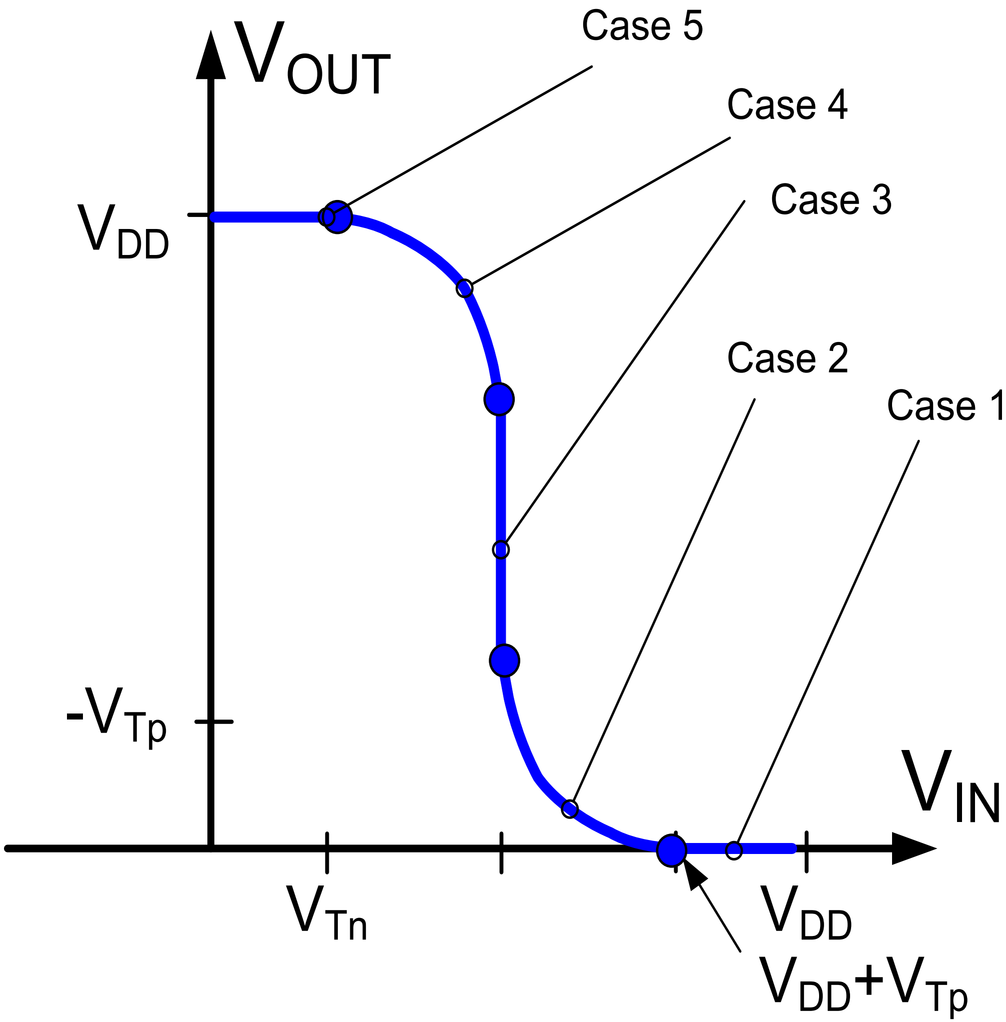
(Neglect λ effects)

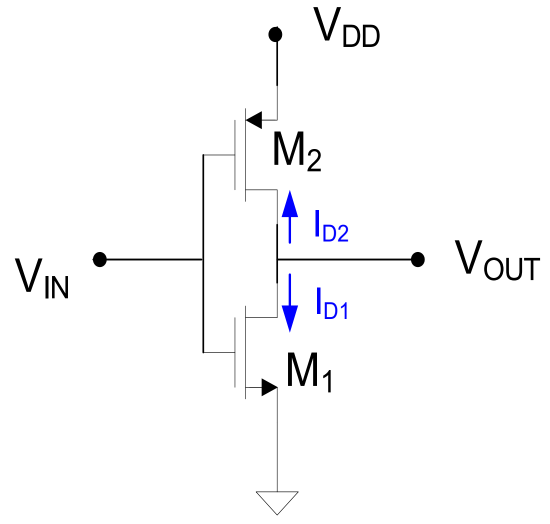
Case 5 M_1 cutoff, M_2 triode



Transfer characteristics of the static CMOS inverter

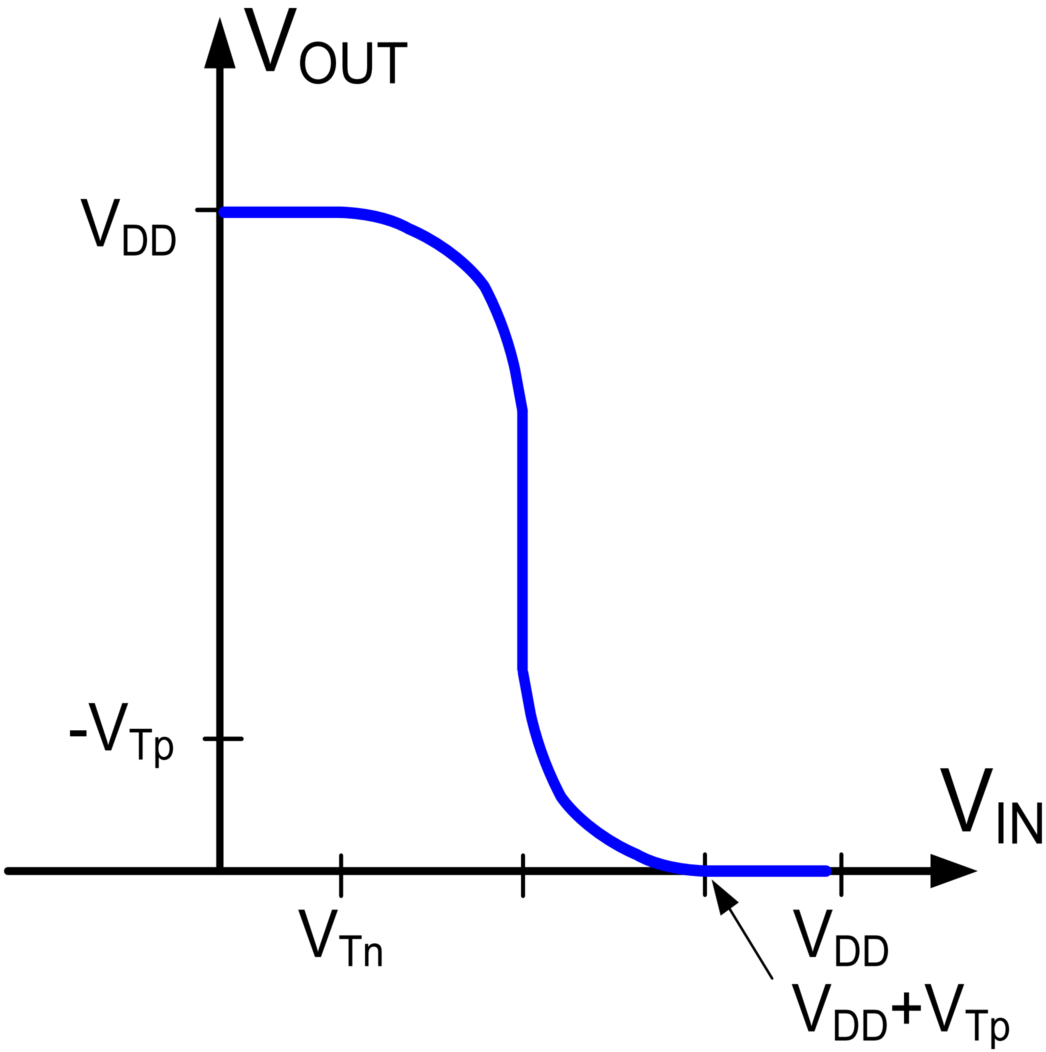
(Neglect λ effects)





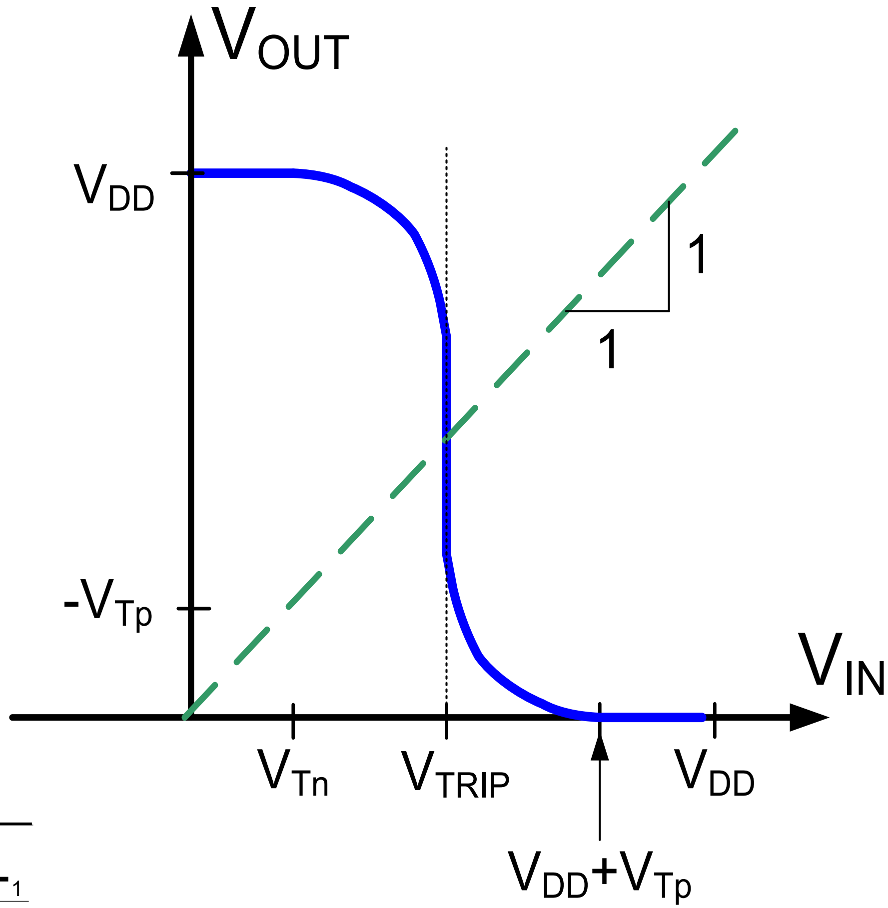
Transfer characteristics of the static CMOS inverter

(Neglect λ effects)



Transfer characteristics of the static CMOS inverter

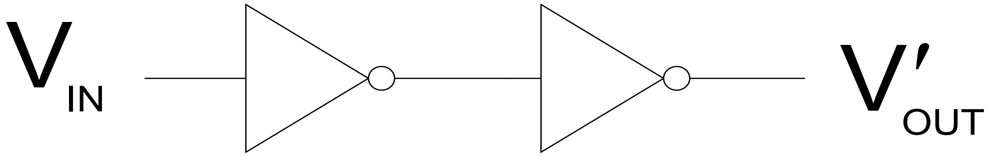
(Neglect λ effects)



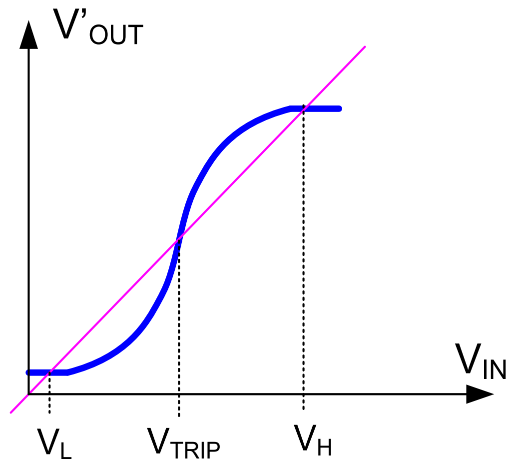
From Case 3 analysis:

$$V_{IN} = \frac{(V_{Tn}) + (V_{DD} + V_{Tp})\sqrt{\frac{\mu_p}{\mu_n}\frac{W_2}{W_1}\frac{L_1}{L_2}}}{1 + \sqrt{\frac{\mu_p}{\mu_n}\frac{W_2}{W_1}\frac{L_1}{L_2}}}$$

Inverter Transfer Characteristics of Inverter Pair

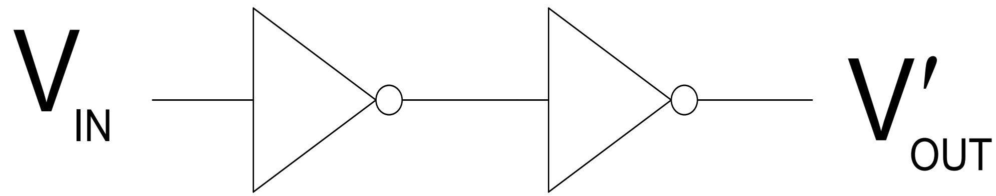


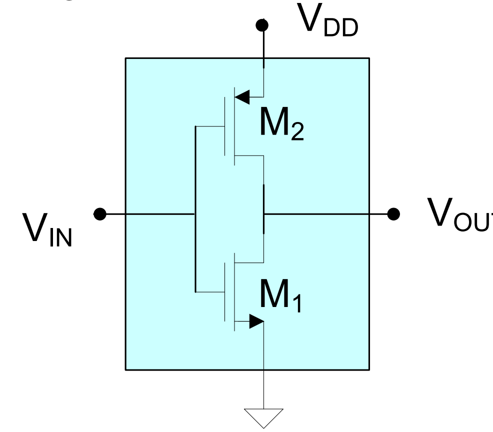
What are V_H and V_L?

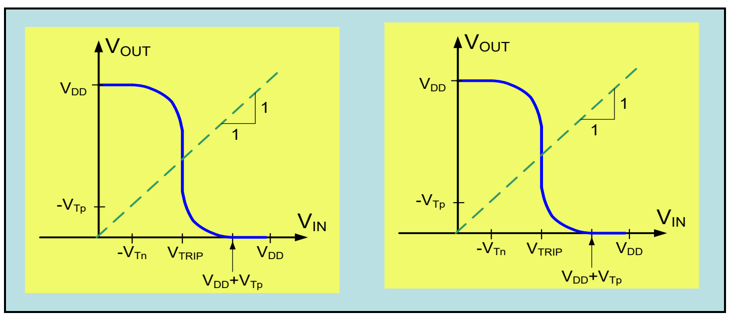


Find the points on the inverter pair transfer characteristics where $V_{OUT}'=V_{IN}$ and the slope is less than 1

Inverter Transfer Characteristics of Inverter Pair for THIS Logic Family



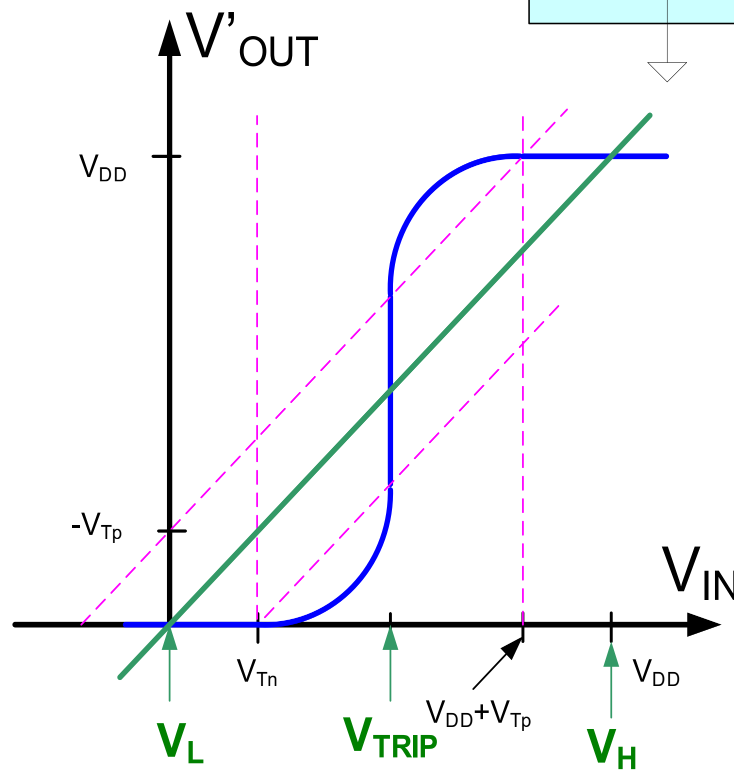




$V_H=V_{DD}$ and $V_L=0$

Note this is independent of device sizing for THIS logic family !!

Designer can use sizing to achieve other desirable properties !!!



Stay Safe and Stay Healthy !

End of Lecture 37